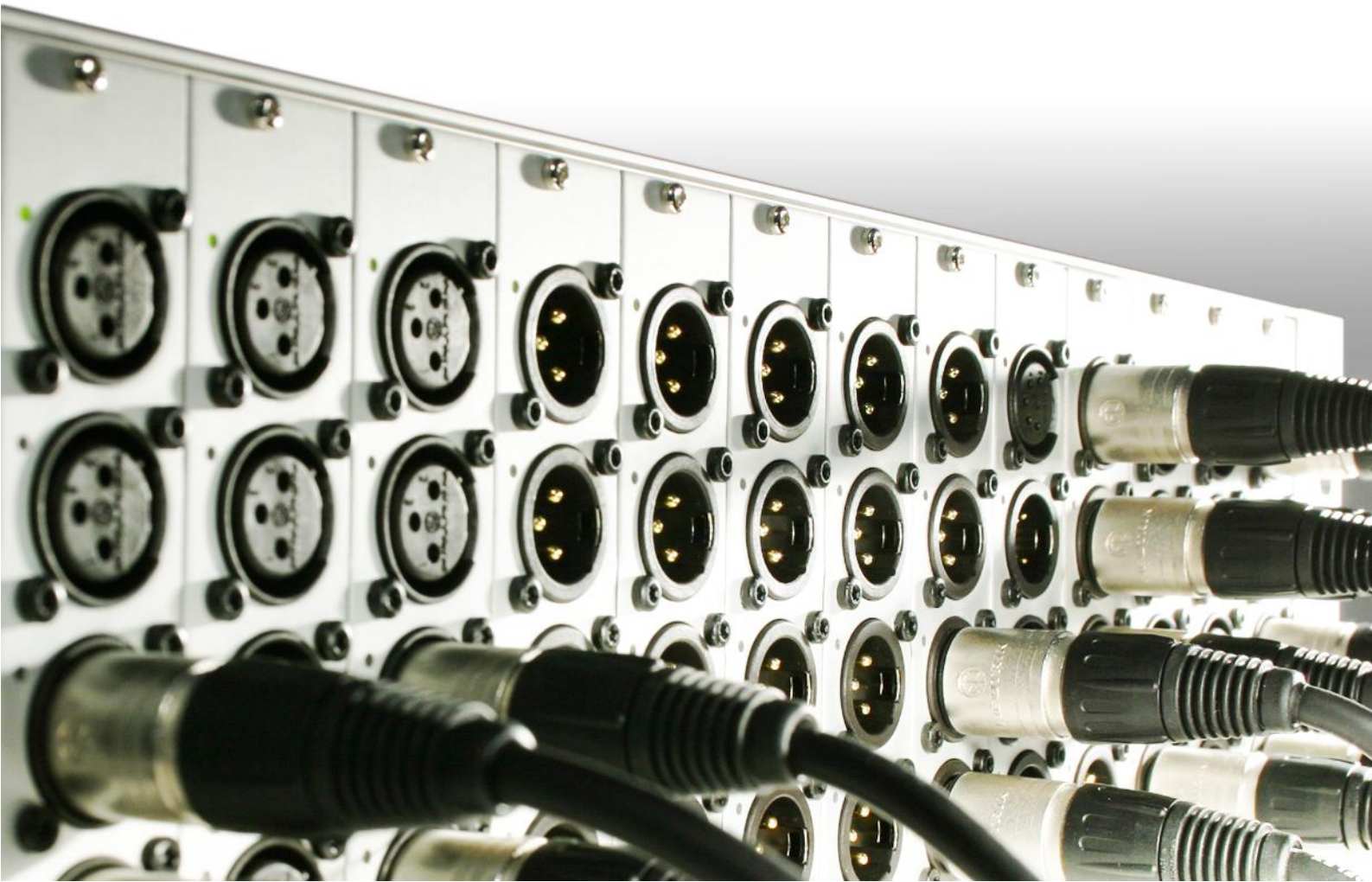
Series 52

52/MB and 52/CR Specifications

Version: 1.14.0



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Terms of Use - Legal Disclaimer

Series 52

52/MB and 52/CR Specifications

Version 1.14.0, 14.04.2010

About this Book

How to Use this Book

The Navigation Tree

You can find the navigation tree on the left-hand-side of the PDF document. Via the entries of this tree you can directly reach the several chapters and sections of this document. Click onto the text or the  symbol of an entry to display its content.

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The Meaning of Advices in the Text

Warning 	The demands and advices in this fields should be followed **unconditional**, because otherwise hardware and software products, data bases, as well as persons may suffer a loss.
Important 	The demands and advices in this fields should be followed, because these contents are necessary for the proper operation of the DHD systems.
Note 	Recommendations and further information are marked as notes. Sometimes you will also find off-topic content in this field, which is related to the actual topic.
Tip 	Tips are helpful advices, which should make work with DHD systems easier.
Weblink 	In this fields you can find links to websites, which include for example an other manual or the possibility to download a driver for the respective DHD system. Please notice, that you need an active internet connection to be able to execute a link to an URL.
Download 	You can directly open and download a file if the respective link is marked as download link (file link).

General Information and Test Conditions

digital reference level:	0 dBFS = digital full scale
analog reference voltage level:	0 dBu = 0.775 V (RMS)
system sampling frequency:	44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz (internal or external)
default system sampling frequency:	48 kHz (internal)
headroom:	adjustable 0 dB ... 30 dB
maximum analog input level:	18 dBu, 24 dBu, 26 dBu (depending on module type)
maximum analog output level:	18 dBu or 24 dBu (depending on module type)
analog source impedance for measurements:	< 40 Ohm
frequency range for measurements:	20 Hz ... 20 kHz (if not stated otherwise)

Note

Please read the 52/MB and 52/CR manuals and the 52/MB and 52/CR lists of modules for further information on the here listed I/O cards.

Audio Latency

In the table below you can find the latencies of single processes inside the 52/MB MADI Breakout System (same values like the 52/CR) and also for the 52/XR MADI Router. Besides, there are listed some total latencies for possible combinations of processes.

Example signal flows:

	Audio Samples	An-Router -An	Dig-Router -An	An-Router -Dig	Dig-Router -Dig	DigSRC-Router -Dig	DigSRC-Router -DigSRC	DigSRC Deemb-Router - DigEmb
Routing Kernel, general latency	4	4	4	4	4	4	4	4
52/MB and 52/CR input, general latency	10	10	10	10	10	10	10	10
52/MB and 52/CR output, general latency	10	10	10	10	10	10	10	10
AD converter CS5361, component dependent latency	12	12		12				
DA converter PCM1793, component dependent latency	29	29	29					
SRC AD1895 input, component dependent latency	48					48	48	48
SRC AD1895 output, component dependent latency	48						48	
SDI embedder, component dependent latency	<48							<48
SDI de-embedder, component dependent latency	<48							<48
total latency in samples (typical)		**65**	**53**	**36**	**24**	**72**	**120**	**<168**
total latency @ 48kHz in ms (typical)		**1.35**	**1.10**	**0.75**	**0.50**	**1.50**	**2.50**	**<3.50**

An-	analog input
Dig-	digital input
DigSRC-	digital input with sample rate converter
DigSRCDeemb-	digital input with sample rate converter and SDI de-embedder
-An	analog output
-Dig	digital output
-DigSRC	digital output with sample rate converter
-DigEmb	digital output with SDI embedder

52-5111A - MB/CR/XD Digital In/Out Module

Technical Specifications

Digital Inputs

input impedance:	110 Ohm (AES3/EBU) or 75Ohm (S/PDIF)
input sensitivity:	> 200mV
input sample rate converters (SRC):	yes, with bypass mode (switchable via browser)
SRC input sampling frequency range:	15 kHz ... 195 kHz (48kHz system frequency)
SRC passband ripple:	< 0.01 dB
dynamic range (SRC off):	144 dB
THD+N (SRC on, 44.1kHz to 48kHz):	< -125 dBFS (-30 dBFS test signal) < -115 dBFS (-1 dBFS test signal)
max. input jitter:	> 40 ns (48kHz system frequency)
supported standards:	AES3/EBU or S/PDIF (switchable via browser)

Digital Outputs

output impedance:	110 Ohm (AES/EBU) or 75Ohm (S/PDIF)
output level:	3.4 V (into 110 Ohm load)
dynamic range (24 bit, dither off):	144dB
dither:	adjustable 16 or 20 bit (triangular shaped)
jitter:	< 2 ns (peak)
supported standards:	AES3/EBU or S/PDIF (switchable via browser)

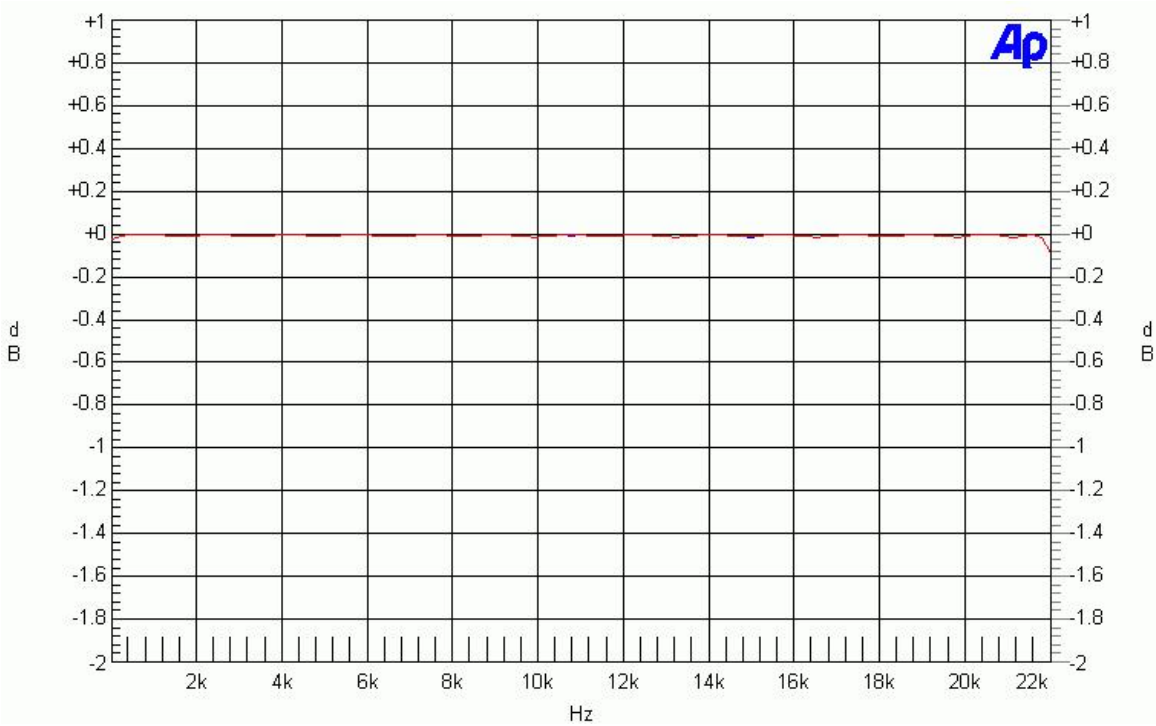
Further Information

power consumption:	1.1 W (typical)
connector style:	XLR 3-pin connectors
printed circuit board (PCB) revision for this specifications:	2

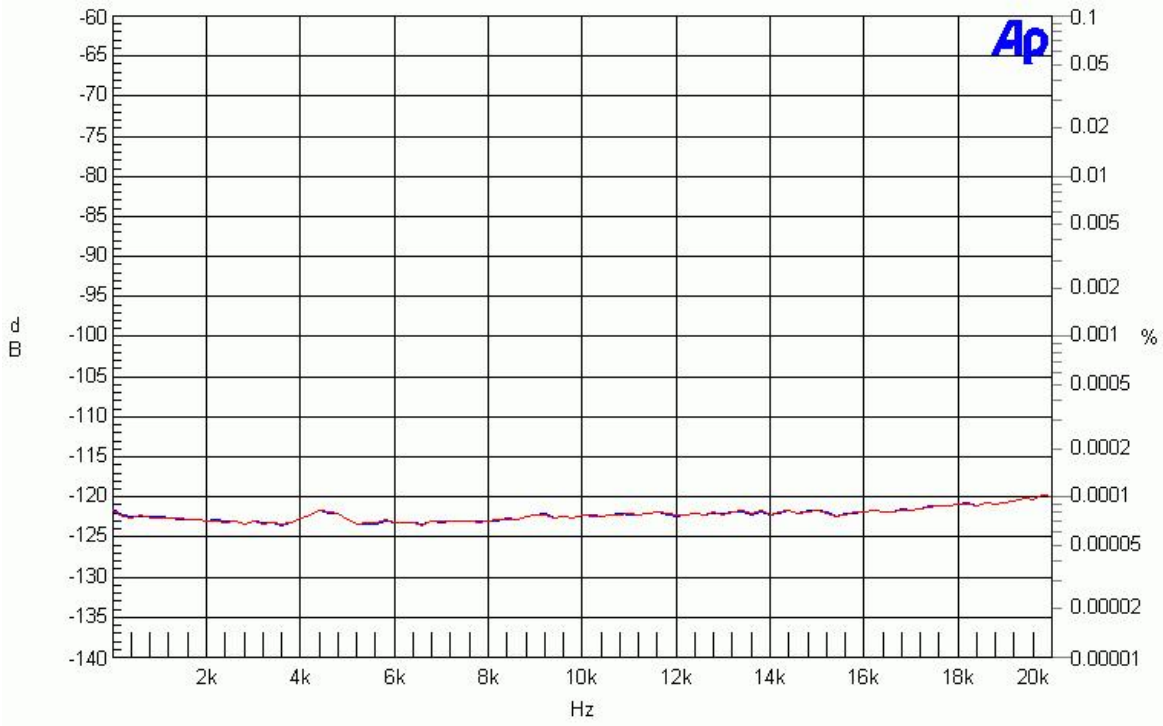
Note

All values are typical values, regarding the factory test limits, you can find in the log file example.

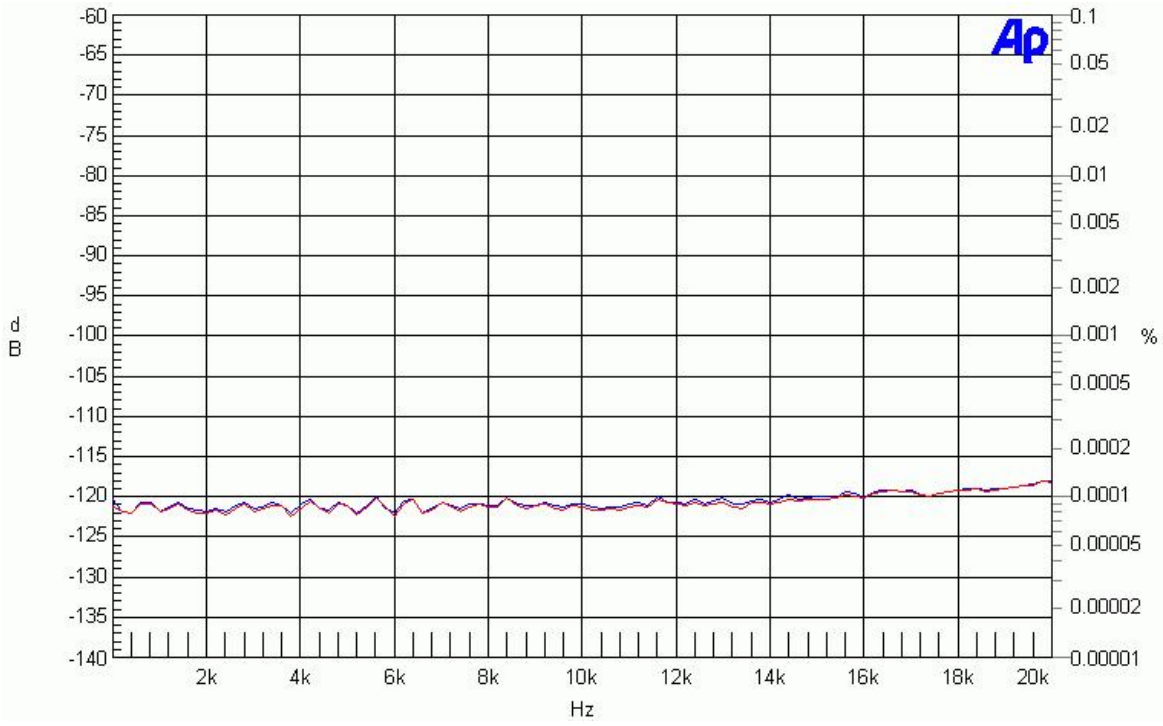
Measurement Plots 52-5111A SRC Inputs



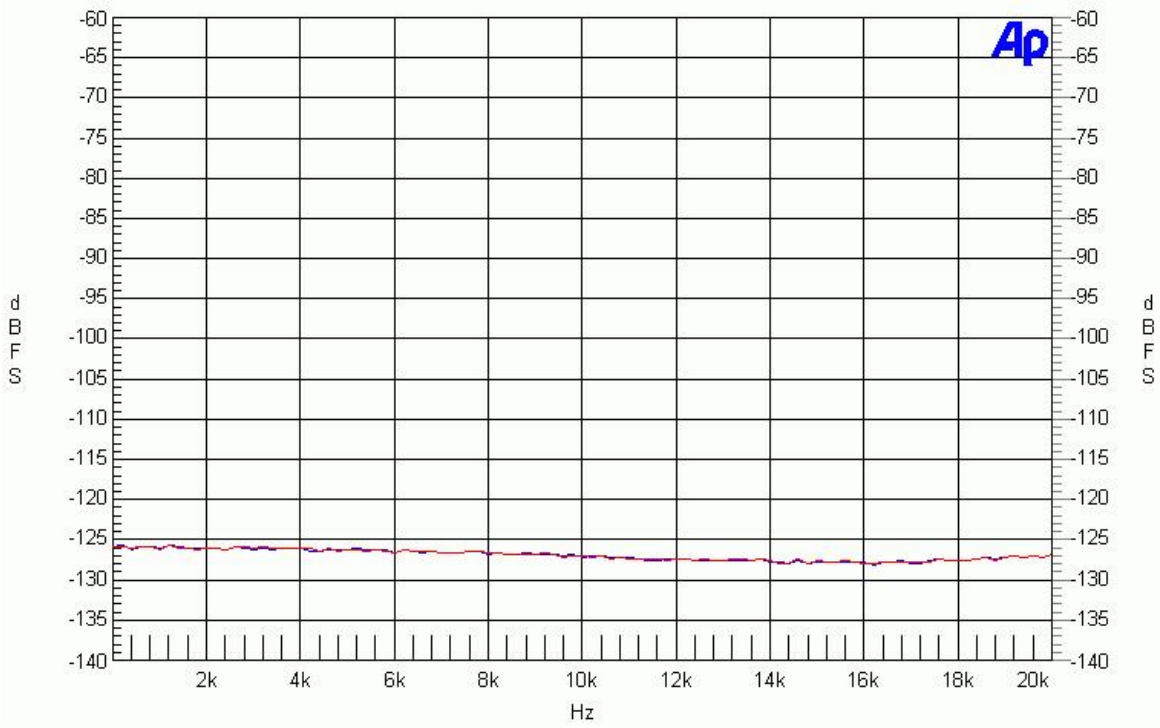
52-5111A Frequency Response, SRC



52-5111A THD+N @ -1 dBFS, SRC 48 kHz to 48 kHz



52-5111A THD+N @ -1 dBFS, SRC 44.1 kHz to 48 kHz



52-5111A THD+N @ -30 dBFS, SRC 44.1 kHz to 48 kHz

Log File Example

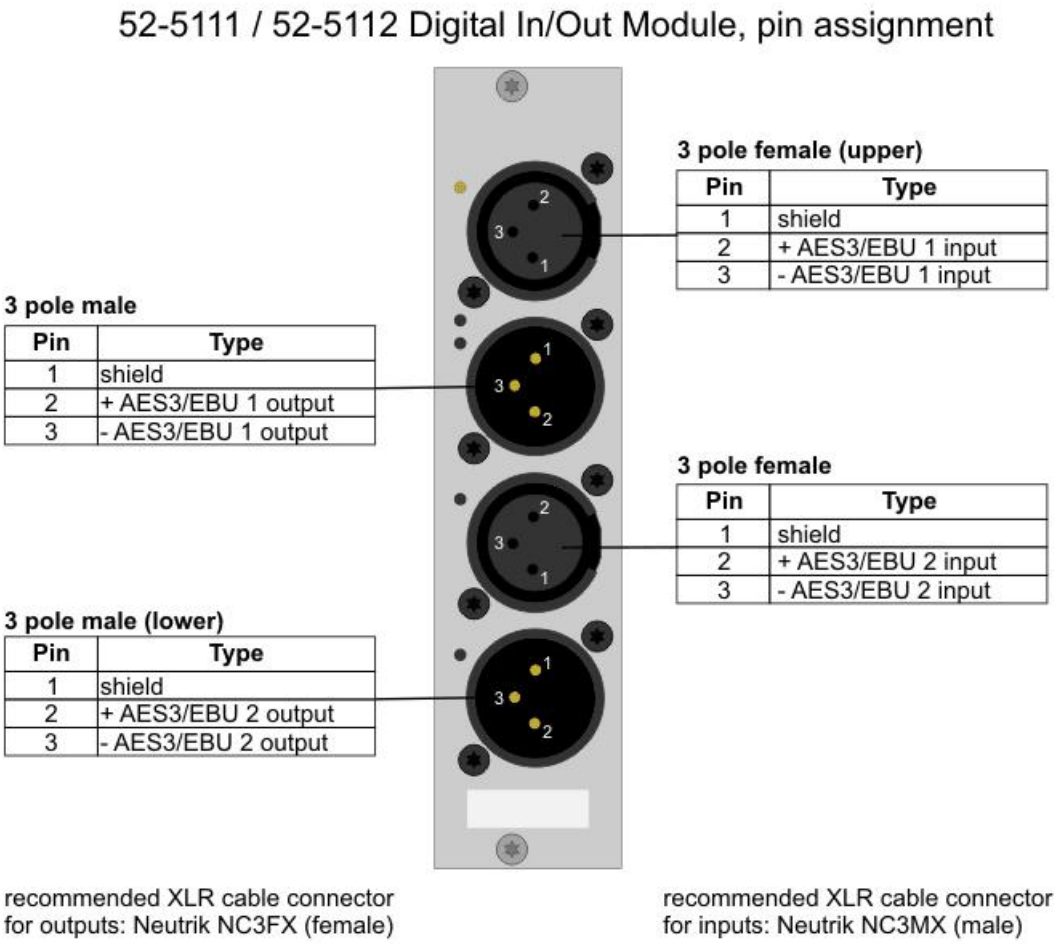
After manufacturing all inputs and outputs of every I/O card are measured. Hence, we can make sure that every module, leaving the production hall, is working correctly. During this process a log file is written. This file is saved by DHD for maintenance purposes.

In the following you can find a log file example of an 52-5111 module:

```
test protocol: z52-51112
serial number: 606836074
production code: 6836
test date: 02-May-2007 13:56:15

input frequency response, SRC off (abs.max. ripple 20Hz..20kHz)
Limit: -0.0001 dB .. +0.0001 dB
  Ch1: 0.000 dB
  Ch2: 0.000 dB
  Ch3: 0.000 dB
  Ch4: 0.000 dB
input frequency response, SRC on (abs.max. ripple 20Hz..20kHz)
Limit: -0.01 dB .. +0.01 dB
  Ch1: 0.012 dB
  Ch2: 0.012 dB
  Ch3: 0.012 dB
  Ch4: 0.012 dB
output frequency response, no SRC (abs.max. ripple 20Hz..20kHz)
Limit: -0.0001 dB .. +0.0001 dB
  Ch1: 0.000 dB
  Ch2: 0.000 dB
  Ch3: 0.000 dB
  Ch4: 0.000 dB
input dynamic range, SRC off:
Limit: +144 dB .. +Inf dB
  Ch1: 145.3 dB
  Ch2: 145.5 dB
  Ch3: 144.9 dB
  Ch4: 145.2 dB
input dynamic range, SRC on:
Limit: +120 dB .. +Inf dB
  Ch1: 124.4 dB
  Ch2: 124.5 dB
```

```
  Ch3: 124.2 dB
  Ch4: 124.1 dB
output dynamic range, no SRC:
Limit: +144 dB .. +Inf dB
  Ch1: 145.1 dB
  Ch2: 145.1 dB
  Ch3: 145.1 dB
  Ch4: 145.0 dB
total group delay (SRC on) @ 48.0kHz:
  TDELAY: 1.16ms (55.6 Samples)
total group delay (SRC off) @ 48.0kHz:
  TDELAY: 0.13ms (6.0 Samples)
power supplies:
  VCC1V2: 1.21 V
  VCC2V5: 2.53 V
  VCC3  : 3.30 V
  VCC5  : 5.02 V
```

Pin Assignment



Pin out for the 52-5111 Module.

52-5112A - MB/CR/XD Digital In/Out Module

Technical Specifications

Digital Inputs

input impedance:	110 Ohm (AES3/EBU) or 75Ohm (S/PDIF)
input sensitivity:	> 200mV
input sample rate converters (SRC):	yes, with bypass mode (switchable via browser)
SRC input sampling frequency range:	15 kHz ... 195 kHz (48kHz system frequency)
SRC passband ripple:	< 0.01 dB
dynamic range (SRC off):	144 dB
THD+N (SRC on, 44.1kHz to 48kHz):	< -125 dBFS (-30 dBFS test signal) < -115 dBFS (-1 dBFS test signal)
max. input jitter:	> 40 ns (48kHz system frequency)
supported standards:	AES3/EBU or S/PDIF (switchable via browser)

Digital Outputs

output impedance:	110 Ohm (AES/EBU) or 75Ohm (S/PDIF)
output level:	3.4 V (into 110 Ohm load)
dynamic range (24 bit, dither off):	144dB
dither:	adjustable 16 or 20 bit (triangular shaped)
jitter:	< 2 ns (peak)
supported standards:	AES3/EBU or S/PDIF (switchable via browser)
output sample rate converters (SRC):	yes, with bypass mode (switchable via browser, synchronized to the input connector above the output connector)

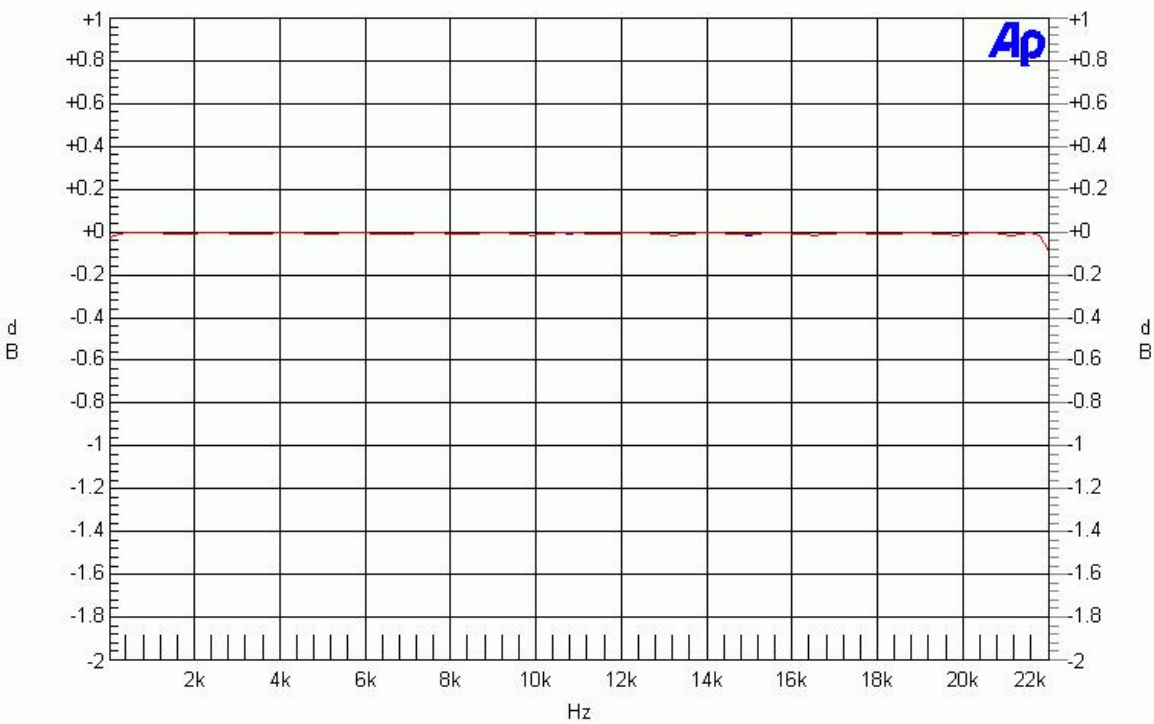
Further Information

power consumption:	1.6 W (typical)
connector style:	XLR 3-pin connectors
printed circuit board (PCB) revision for this specifications:	2

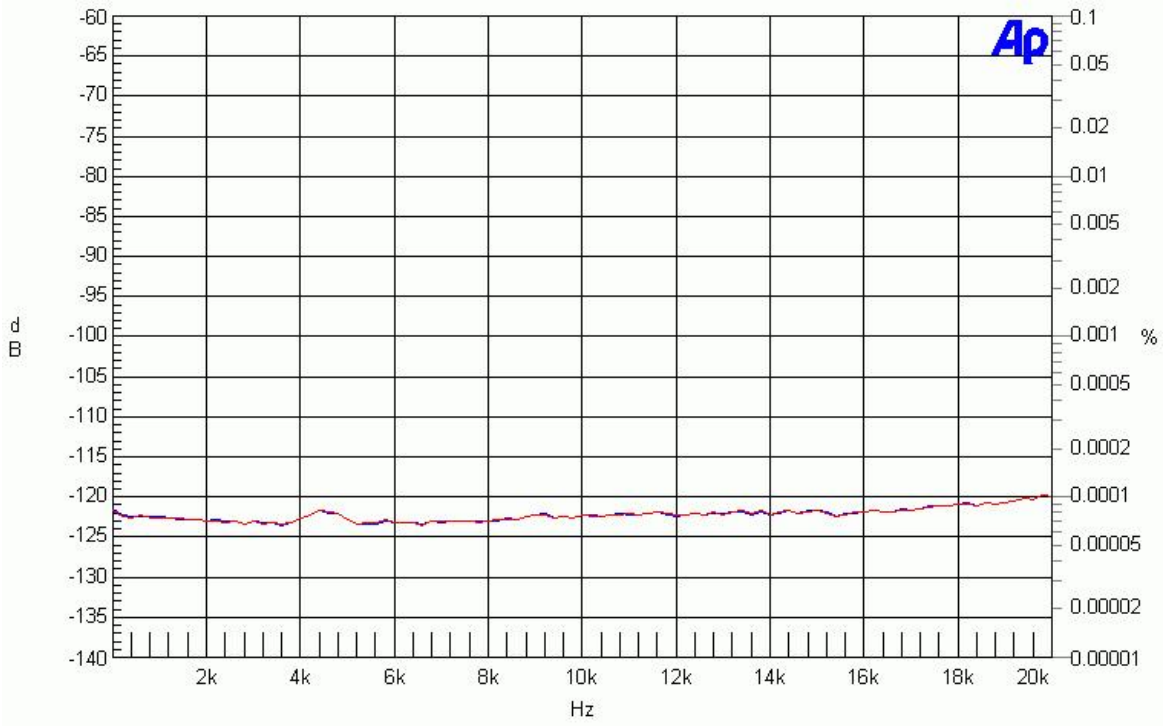
Note

All values are typical values, regarding the factory test limits, you can find in the log file example.

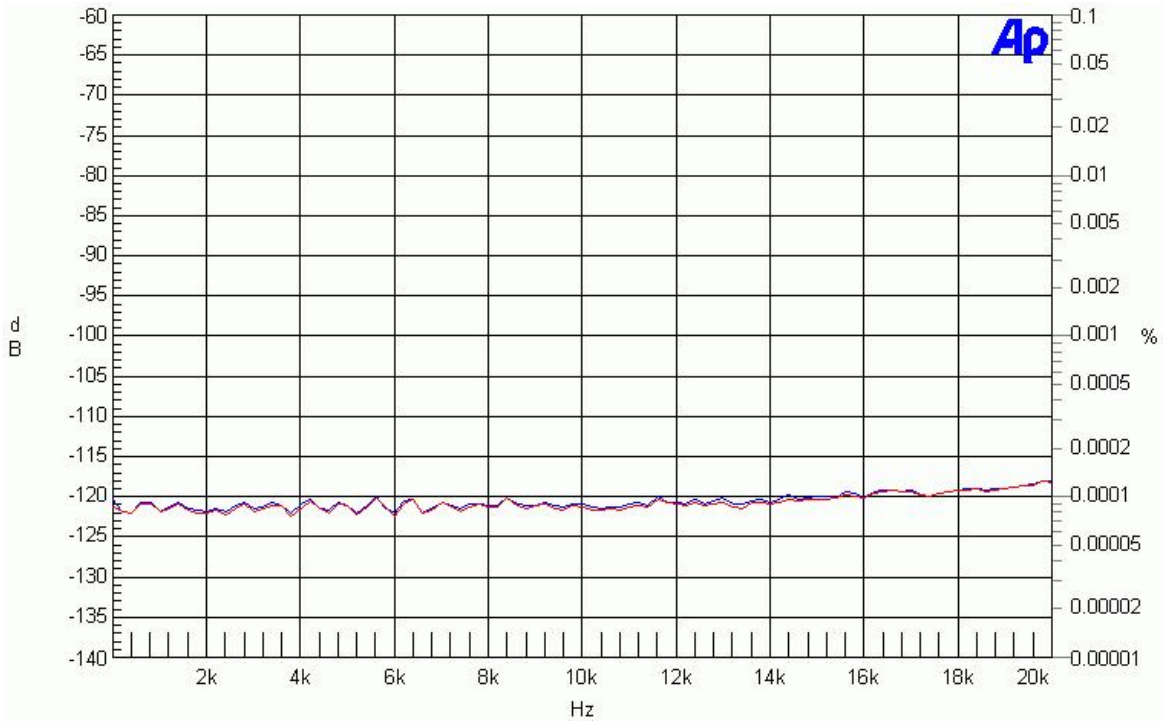
Measurement Plots 52-5112A SRC Inputs



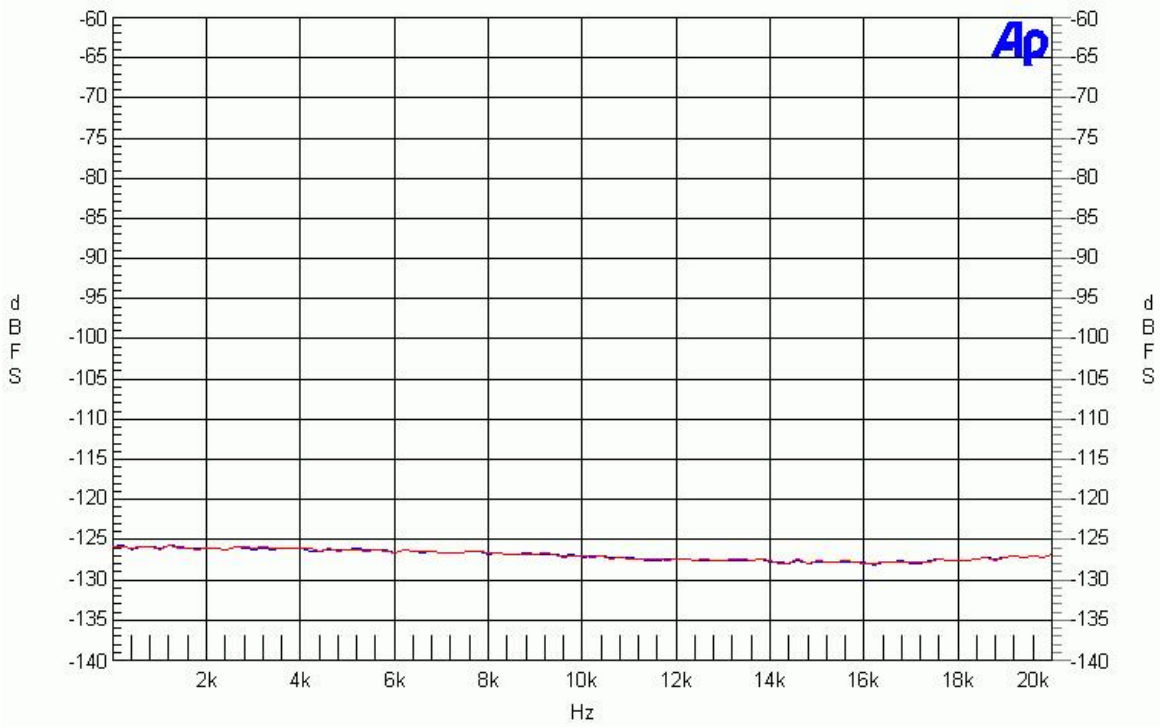
52-5112A Frequency Response, SRC



52-5112A THD+N @ -1 dBFS, SRC 48 kHz to 48 kHz



52-5112A THD+N @ -1 dBFS, SRC 44.1 kHz to 48 kHz



52-5112A THD+N @ -30 dBFS, SRC 44.1 kHz to 48 kHz

Log File Example

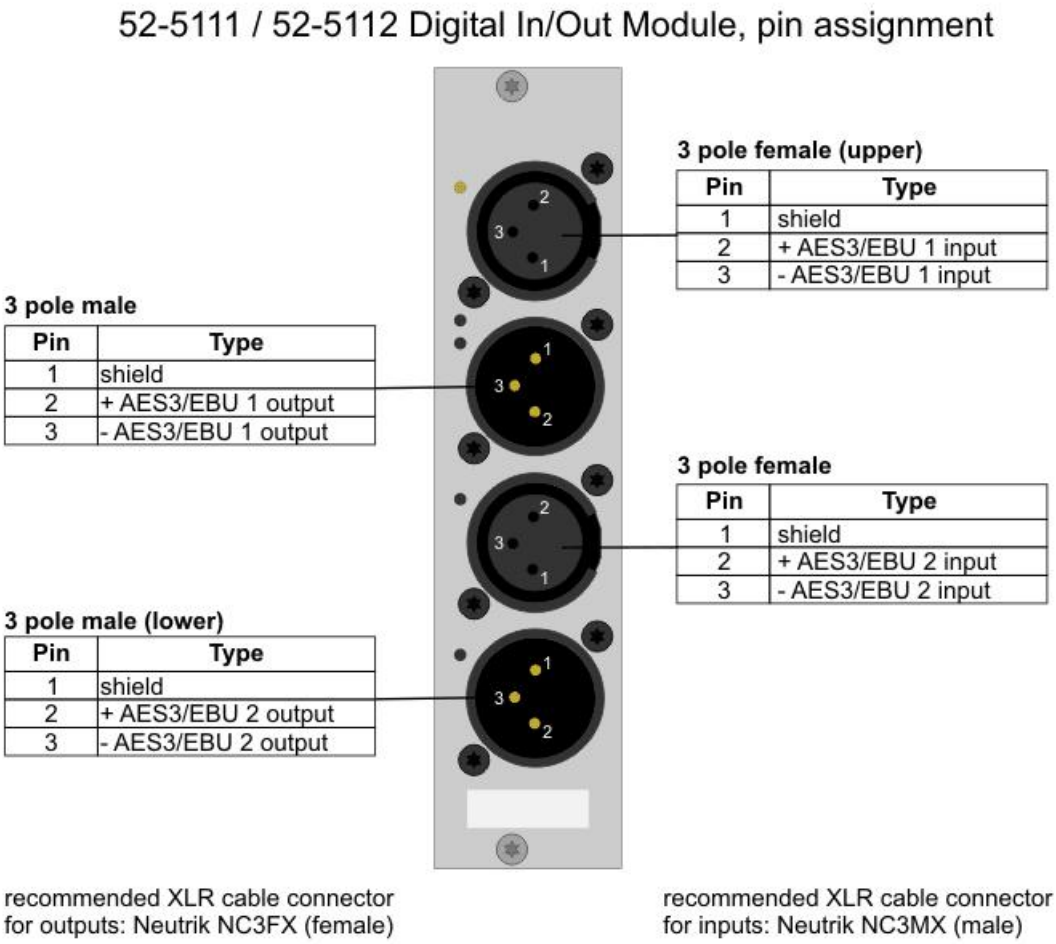
After manufacturing all inputs and outputs of every I/O card are measured. Hence, we can make sure that every module, leaving the production hall, is working correctly. During this process a log file is written. This file is saved by DHD for maintenance purposes.

In the following you can find a log file example of an 52-5112 module:

```
test protocol: z52-51122
serial number: 606836074
production code: 6836
test date: 02-May-2007 13:56:15

input frequency response, SRC off (abs.max. ripple 20Hz..20kHz)
Limit: -0.0001 dB .. +0.0001 dB
  Ch1: 0.000 dB
  Ch2: 0.000 dB
  Ch3: 0.000 dB
  Ch4: 0.000 dB
input frequency response, SRC on (abs.max. ripple 20Hz..20kHz)
Limit: -0.01 dB .. +0.01 dB
  Ch1: 0.012 dB
  Ch2: 0.012 dB
  Ch3: 0.012 dB
  Ch4: 0.012 dB
output frequency response, no SRC (abs.max. ripple 20Hz..20kHz)
Limit: -0.0001 dB .. +0.0001 dB
  Ch1: 0.000 dB
  Ch2: 0.000 dB
  Ch3: 0.000 dB
  Ch4: 0.000 dB
input dynamic range, SRC off:
Limit: +144 dB .. +Inf dB
  Ch1: 145.3 dB
  Ch2: 145.5 dB
  Ch3: 144.9 dB
  Ch4: 145.2 dB
input dynamic range, SRC on:
Limit: +120 dB .. +Inf dB
  Ch1: 124.4 dB
  Ch2: 124.5 dB
```

```
  Ch3: 124.2 dB
  Ch4: 124.1 dB
output dynamic range, no SRC:
Limit: +144 dB .. +Inf dB
  Ch1: 145.1 dB
  Ch2: 145.1 dB
  Ch3: 145.1 dB
  Ch4: 145.0 dB
total group delay (SRC on) @ 48.0kHz:
  TDELAY: 1.16ms (55.6 Samples)
total group delay (SRC off) @ 48.0kHz:
  TDELAY: 0.13ms (6.0 Samples)
power supplies:
  VCC1V2: 1.21 V
  VCC2V5: 2.53 V
  VCC3  : 3.30 V
  VCC5  : 5.02 V
```

Pin Assignment



Pin out for the 52-5112 Module.

52-5170A - MB/CR/XD HD-SDI Audio Module

Technical Specifications

SD-SDI

SD-SDI (SMPTE-259M): Used to transport uncompressed standard-definition digital video.

> **Note**
>
> The 52-5170 module only supports 270MBit/s data rate, PAL and NTSC format!

HD-SDI

HD-SDI (SMPTE-292M): Used to transport uncompressed high-definition digital video.

SMPTE Standard	260M		295M	274M								296M	
Format Designation	**A**	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**I**	**J**	**K**	**L**	**M**
Format (1)	1035i	1035i	1080i	1080i	1080i	1080i	1080p	1080p	1080p	1080p	1080p	720p	720p
Frame Rate (Hz)	30	30/M	25	30	30/M	25	30	30/M	25	24	24/M	60	60/M
Sample Rate (MHz)	74.25	74.25/M	74.25	74.25	74.25/M	74.25	74.25	74.25/M	74.25	74.25	74.25/M	74.25	74.25/M
Active Samples per Line and Active Lines per Frame (words x lines) (2)	1920 x 1035	1920 x 1035	1920 x 1080	1920 x 1080	1920 x 1080	1920 x 1080	1920 x 1080	1920 x 1080	1920 x 1080	1920 x 1080	1920 x 1080	1280 x 720	1280 x 720
Total Samples per Line and Total Lines per Frame (words x lines) (2)	2200 x 1125	2200 x 1125	2376 x 1250	2200 x 1125	2200 x 1125	2640 x 1125	2200 x 1125	2200 x 1125	2640 x 1125	2750 x 1125	2750 x 1125	1650 x 750	1650 x 750

HD-SDI Compatible Video Formats from SMPTE 292M

(1) The format designations follow the industry practice of using the number of active lines per frame plus either the letter "i" indicating interlaced scan or the letter "p" indicating progressive scan. Thus, a format listed as 1080i has 1080 active lines per frame and is interlaced, while a format given as 720p has 720 active lines per frame and is progressive scan.

(2) The active samples per line and total samples per line shown are 2-word samples, one word of Y and one word of C. If there are 1920 active samples in a line, then there are 3840 10-bit active words per line after the channels have been interleaved.

Digital Audio Specifications

input sample rate converters (SRC):	yes, with bypass mode (switchable via browser)
SRC input sampling frequency range:	32 kHz ... 96 kHz
THD+N (SRC on, 44.1kHz to 48kHz):	< -130 dBFS (-1 dBFS test signal, 24 bit audio data) < -121 dBFS (-1 dBFS test signal, 20 bit audio data)
dynamic range:	140 dB (24 bit audio data) 121 dB (20 bit audio data)
SRC passband ripple:	< 0.01 dB
delay configurable per channel pair	0 ... 10 sec
digital gain configurable per channel pair	-20 ... +6 dB

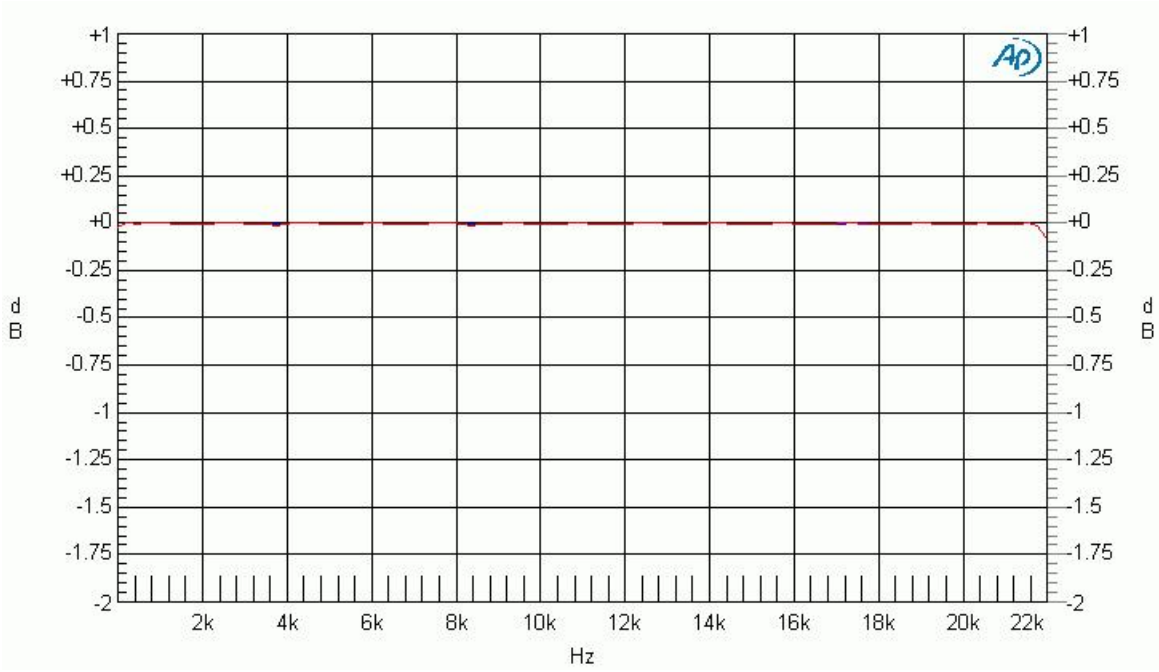
Further Information

power consumption:	3 W (typical)
connector style:	BNC
printed circuit board (PCB) revision for this specifications:	1

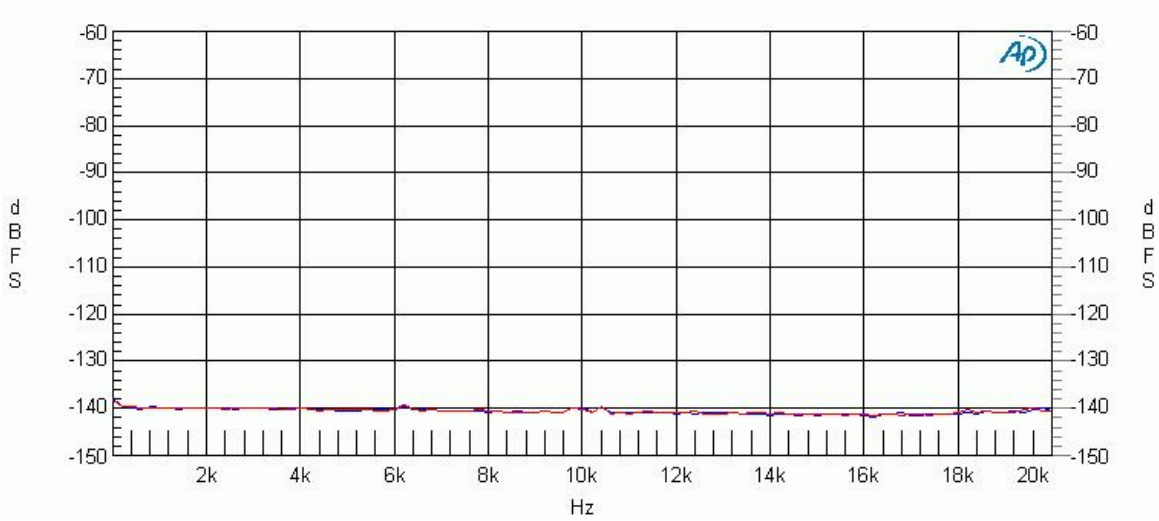
Note

All values are typical values, regarding the factory test limits, you can find in the log file example.

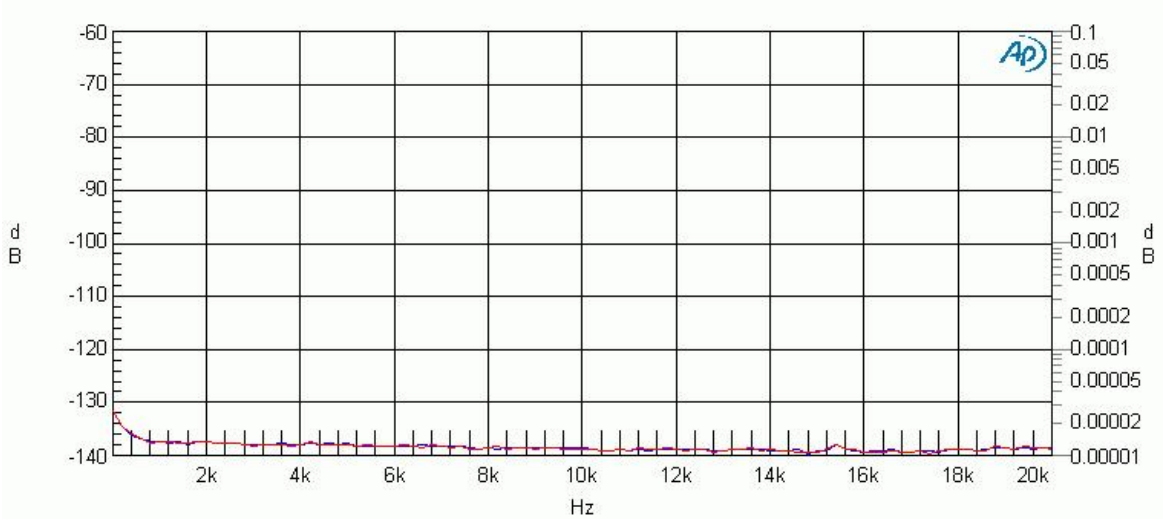
Measurement Plots 52-5170A



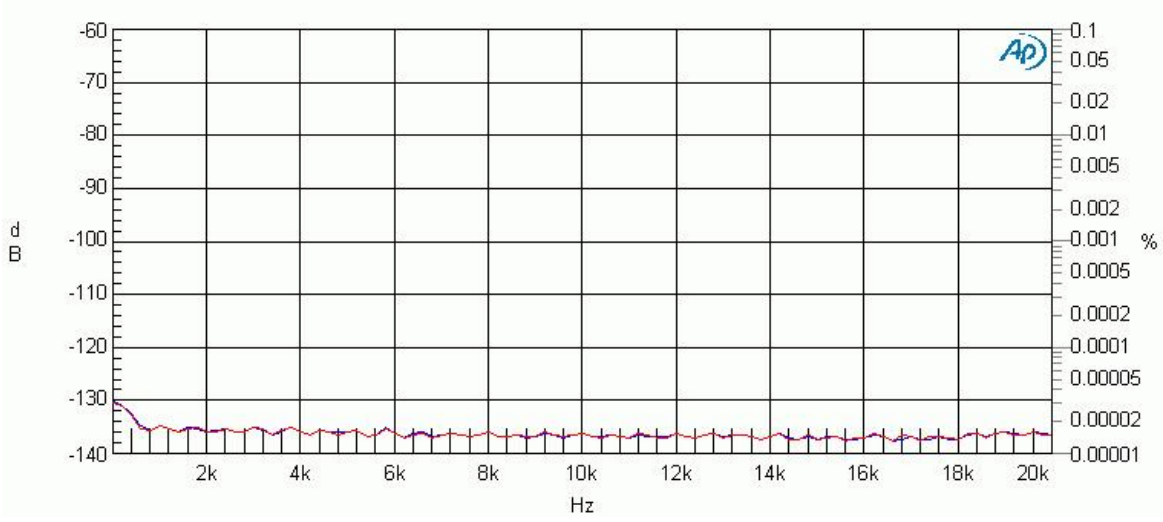
52-5170A Frequency Response, SRC 48 kHz to 48 kHz



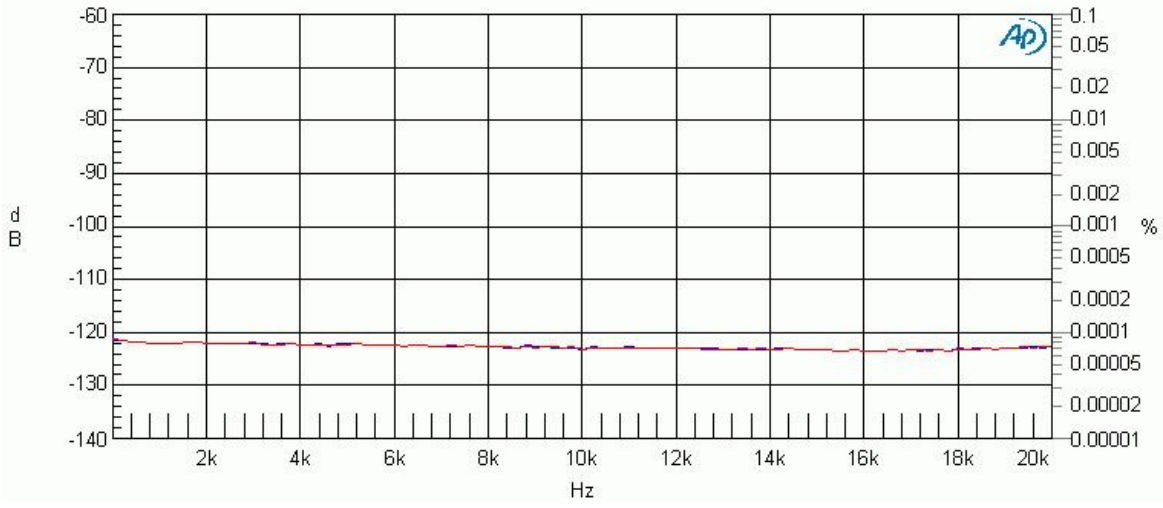
52-5170A THD+N @ -30 dBFS, SRC 44.1 kHz to 48 kHz



52-5170A THD+N @ -1 dBFS, SRC 48 kHz to 48 kHz



52-5170A THD+N @ -1 dBFS, SRC 44.1 kHz to 48 kHz



52-5170A THD+N @ -1 dBFS, SRC 44.1 kHz to 48 kHz (SD-625 20 bit audio data)

Log File Example

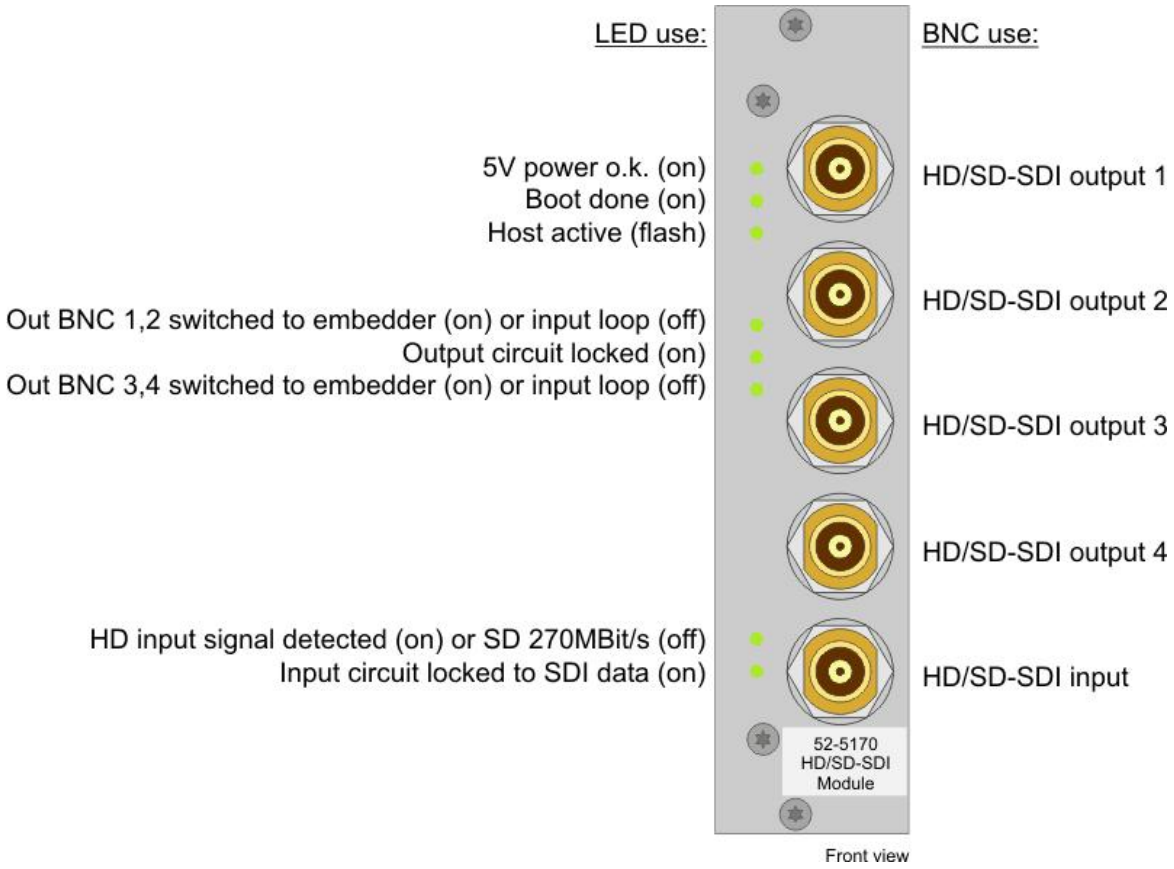
After manufacturing all inputs and outputs of every I/O card are measured. Hence, we can make sure that every module, leaving the production hall, is working correctly. During this process a log file is written. This file is saved by DHD for maintenance purposes.

In the following you can find a log file example of an 52-5170 module:

```
*** Factory Test z52-51701 ***

=== Embedder BNC Output 1 Ch.1:2 ===
Gain(1kHz): L=-0.01 dB,  R=-0.01 dB
Polarity: (+)
total group delay @ 48.0kHz: L=2.89ms,  R=2.89ms (L=138.8,  R=138.8 Samples)
ripple (20Hz..20000Hz) L=0.045 dB, R=0.046 dB
!!! minimum limit violation (amplitude < -0.02 dB))
dynamic:  L=39.3 dB,     R=39.3 dB
!!! limit violation (dynamic < 60 dB))
Gain(1kHz): L=-0.01 dB,  R=-0.01 dB
Polarity: (+)
total group delay @ 48.0kHz: L=2.89ms,  R=2.89ms (L=138.7,  R=138.7 Samples)
ripple (20Hz..20000Hz) L=0.024 dB, R=0.024 dB
dynamic:  L=73.9 dB,     R=73.9 dB

=== Embedder BNC Output 2 Ch.3:4 ===
Gain(1kHz): L=-0.01 dB,  R=-0.01 dB
Polarity: (+)
total group delay @ 48.0kHz: L=2.88ms,  R=2.88ms (L=138.2,  R=138.2 Samples)
ripple (20Hz..20000Hz) L=0.039 dB, R=0.040 dB
!!! minimum limit violation (amplitude < -0.02 dB))
dynamic:  L=40.4 dB,     R=40.4 dB
!!! limit violation (dynamic < 60 dB))
Gain(1kHz): L=-0.01 dB,  R=-0.01 dB
Polarity: (+)
total group delay @ 48.0kHz: L=2.88ms,  R=2.88ms (L=138.1,  R=138.1 Samples)
ripple (20Hz..20000Hz) L=0.024 dB, R=0.024 dB
dynamic:  L=72.6 dB,     R=72.6 dB

=== Embedder Test BNC Output 3 Ch.5:6 ===
5. Prüfling 5170 Slot 2 BNC Output 3 (3. von oben) mit Testkarte 5170 Slot 1 Input (unten) verbinden
Gain(1kHz): L=-0.01 dB,  R=-0.01 dB
Polarity: (+)
total group delay @ 48.0kHz: L=3.22ms,  R=3.22ms (L=154.4,  R=154.4 Samples)
ripple (20Hz..20000Hz) L=0.064 dB, R=0.066 dB
!!! minimum limit violation (amplitude < -0.02 dB))
dynamic:  L=36.3 dB,     R=36.3 dB
!!! limit violation (dynamic < 60 dB))
Gain(1kHz): L=-0.01 dB,  R=-0.01 dB
Polarity: (+)
total group delay @ 48.0kHz: L=3.21ms,  R=3.21ms (L=154.3,  R=154.3 Samples)
ripple (20Hz..20000Hz) L=0.024 dB, R=0.024 dB
dynamic:  L=73.5 dB,     R=73.5 dB

=== Embedder Test BNC Output 4 Ch.7:8 ===
Gain(1kHz): L=-0.01 dB,  R=-0.01 dB
Polarity: (+)
total group delay @ 48.0kHz: L=3.21ms,  R=3.21ms (L=153.9,  R=153.9 Samples)
ripple (20Hz..20000Hz) L=0.037 dB, R=0.036 dB
!!! minimum limit violation (amplitude < -0.02 dB))
dynamic:  L=41.4 dB,     R=41.4 dB
!!! limit violation (dynamic < 60 dB))
Gain(1kHz): L=-0.01 dB,  R=-0.01 dB
Polarity: (+)
total group delay @ 48.0kHz: L=3.21ms,  R=3.21ms (L=153.9,  R=153.9 Samples)
ripple (20Hz..20000Hz) L=0.024 dB, R=0.024 dB
dynamic:  L=81.1 dB,     R=81.1 dB

=== HD-SDI Test 720p50 ===
e2 =
     0
e1 =
     0

passed.

=== Write EEPROM ===
new serial number: 708272001
reading old IDs:
```

```
  type: 5170
  Xilinx bitfile: 5170
  hardware revision: 255
  production code: 65535
  serial number: 4.294967e+009
  test date: 07-Feb-2006 06:28:15
writing new IDs:
  type: 5170
  Xilinx bitfile: 5170
  hardware revision: 1
  production code: 8272
  serial number: 708272001
  test date: 12-Nov-2007 08:51:03
elapsed_time =
       78.109
```

Pin Assignment



Pin out for the 52-5170 Module.

52-5210A - MB/CR/XD 4 Ch. Line In, 18dBu

Technical Specifications

A/D Converter

max. input level:	18 dBu (balanced)
input impedance:	approx. 10 kOhm
frequency response:	< 0.1 dB
THD+N:	< -107 dBFS (-30 dBFS, -15 dBu test signal level)
	< -105 dBFS (-9 dBFS, +6 dBu test signal level)
	< -95 dBFS (-1 dBFS, +14 dBu test signal level)
crosstalk:	< -110 dB (1kHz)
dynamic range:	110dB (A-weighted, 0 dBFS = +15 dBu)
common mode rejection:	> 60 dB
converter technology:	24 bit, oversampling sigma-delta

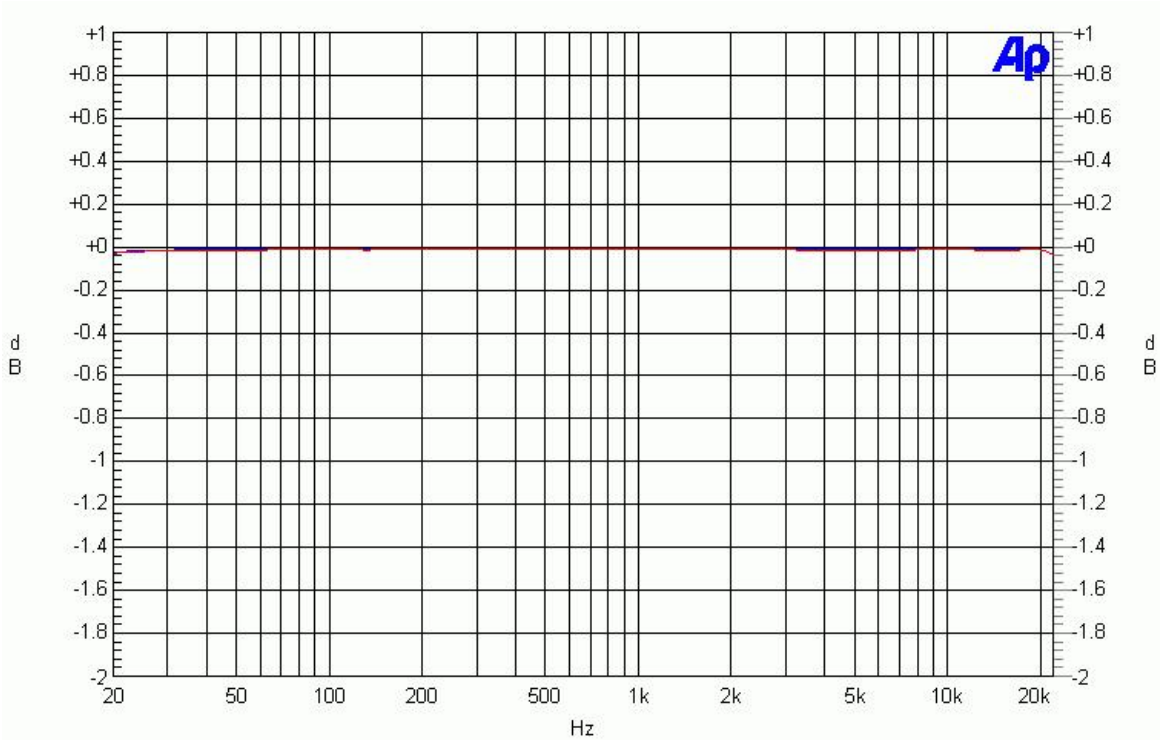
Further Information

power consumption:	1.7 W (typical)
connector style:	XLR 3-pin connectors
printed circuit board (PCB) revision for this specifications:	1

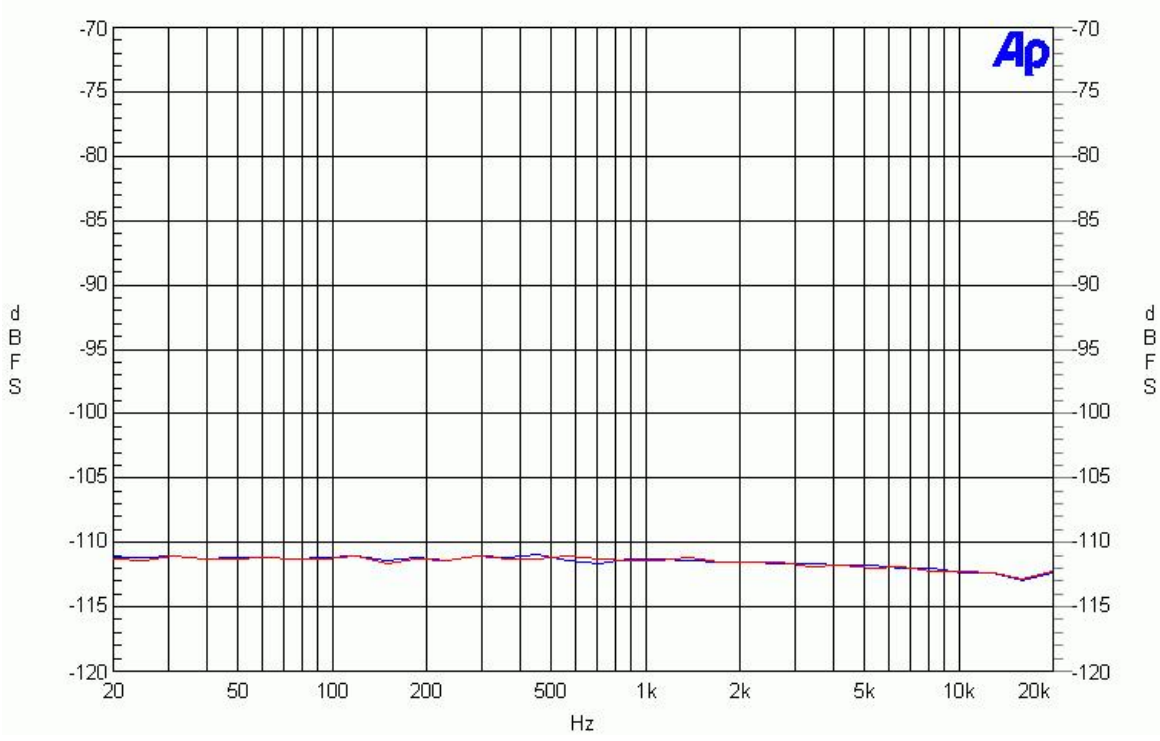
Note

All values are typical values, regarding the factory test limits.

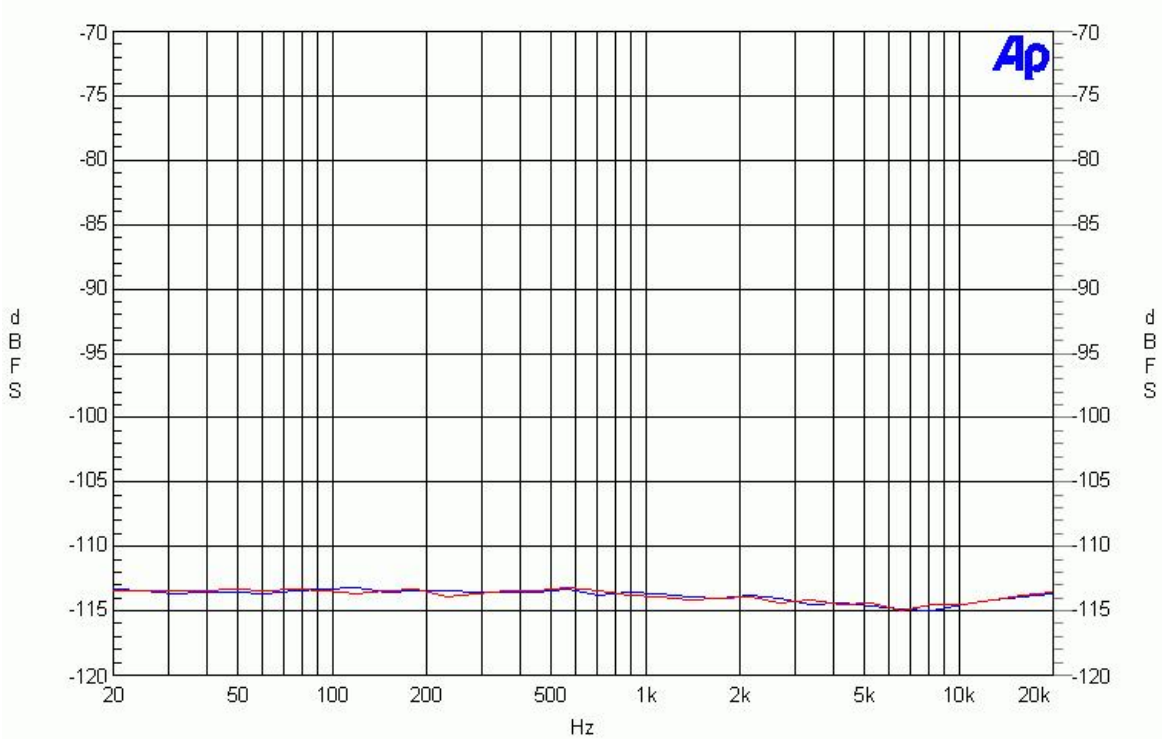
Measurement Plots 52-5210A



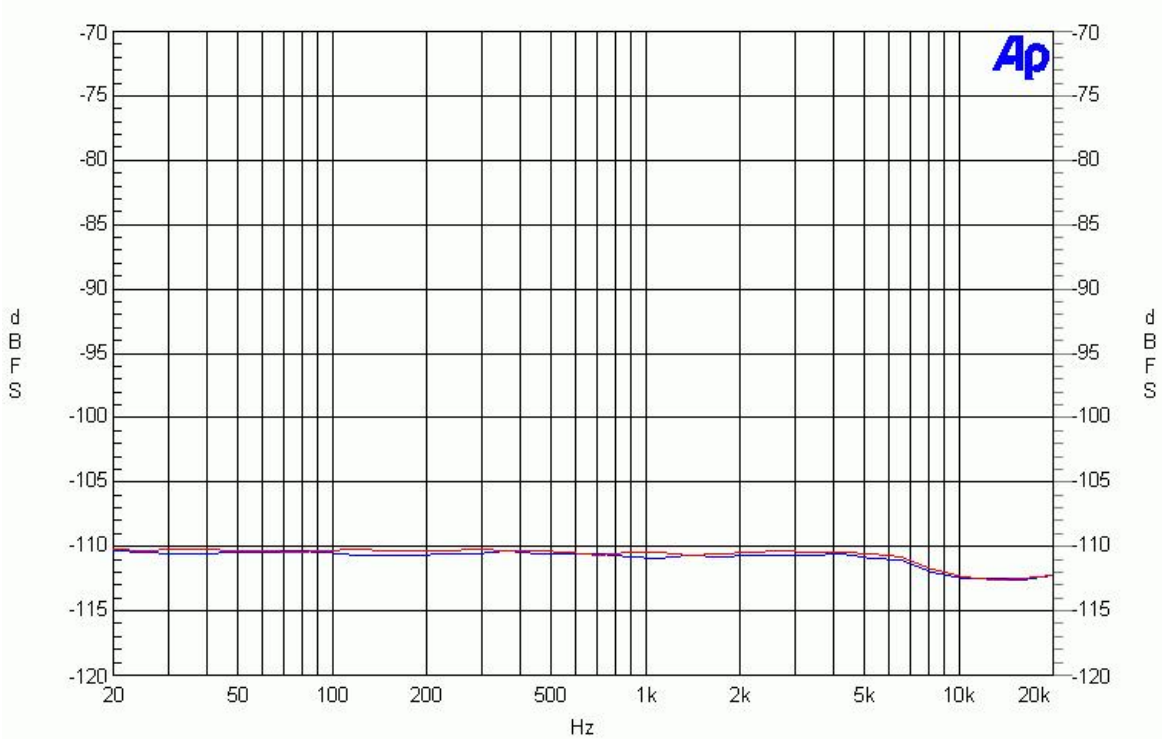
52-5210A ADC Frequency Response



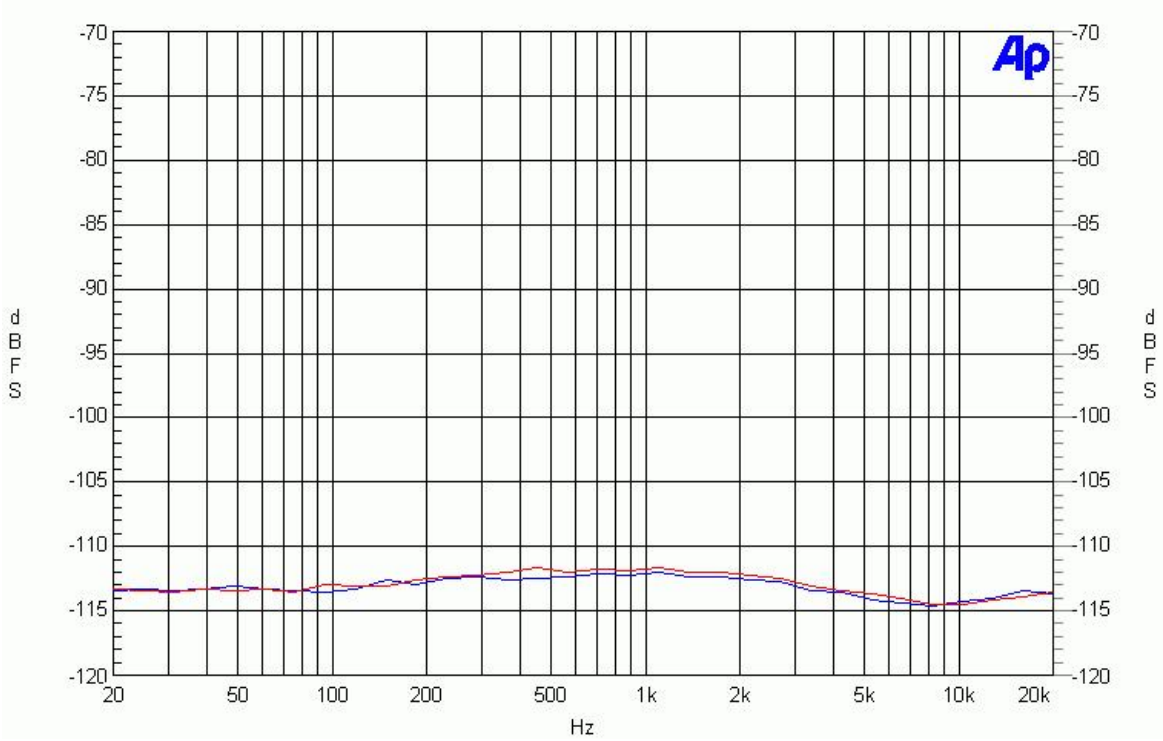
52-5210A ADC THD+N @ -30 dBFS



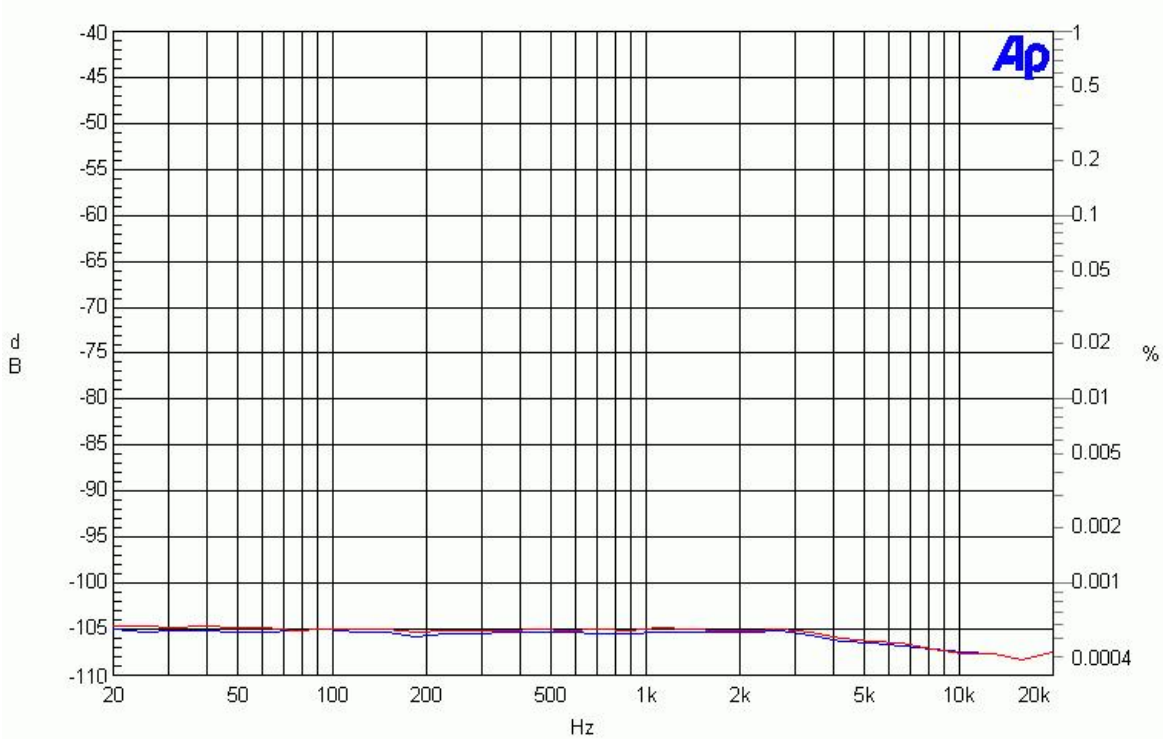
52-5210A ADC THD+N(A) @ -30 dBFS



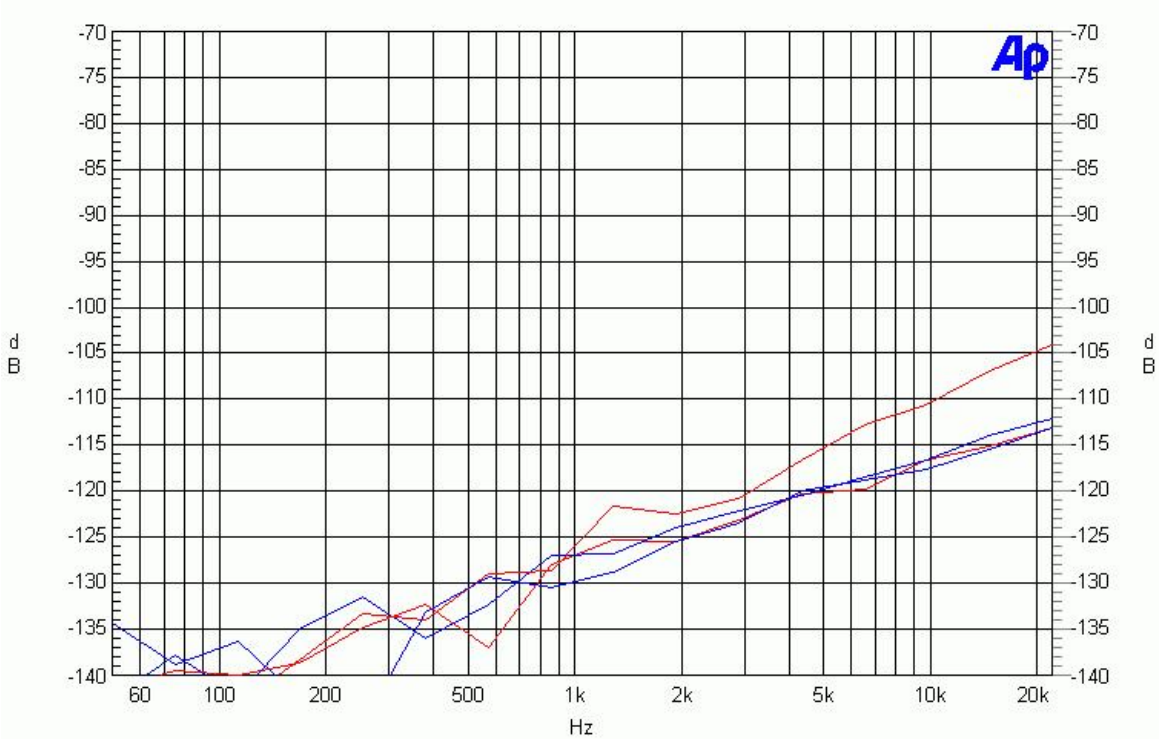
52-5210A ADC THD+N @ +6 dBu



52-5210A ADC THD+N(A) @ + 6 dBu

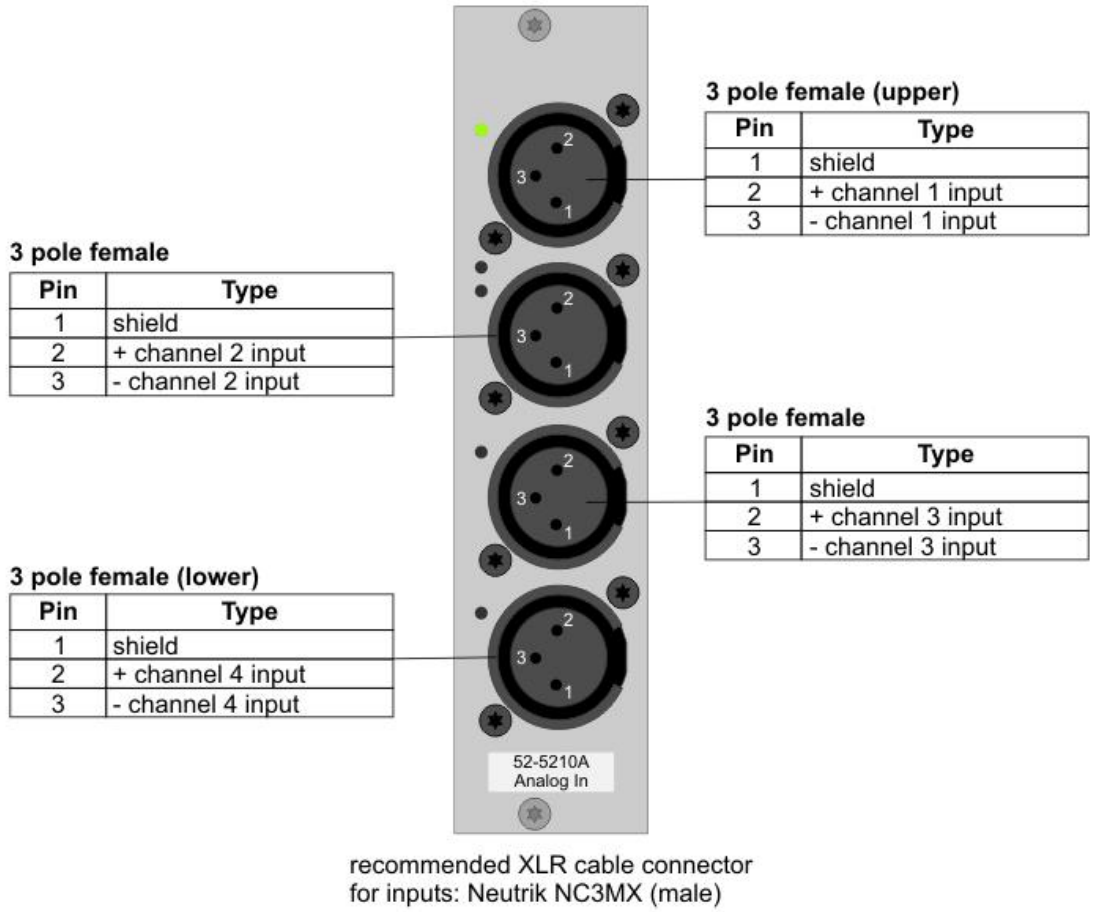


52-5210A ADC THD+N @ +14 dBu



52-5210A ADC Cross-Talk

Pin Assignment



Pin out for the 52-5210 Module.

52-5213A - MB/CR/XD 4 Ch. Line In, 24dBu

Technical Specifications

A/D Converter

max. input level:	24 dBu (balanced)
input impedance:	approx. 10 kOhm
frequency response:	< 0.1 dB
THD+N:	< -110 dBFS (-30 dBFS, -6 dBu test signal level)
	< -110 dBFS (-20 dBFS, +4 dBu test signal level)
	< -90 dBFS (-1 dBFS, +23 dBu test signal level)
crosstalk:	< -110 dB
dynamic range:	113 dB (A-weighted, 0 dBFS = +24 dBu)
common mode rejection:	> 60 dB
converter technology:	24 bit, oversampling sigma-delta

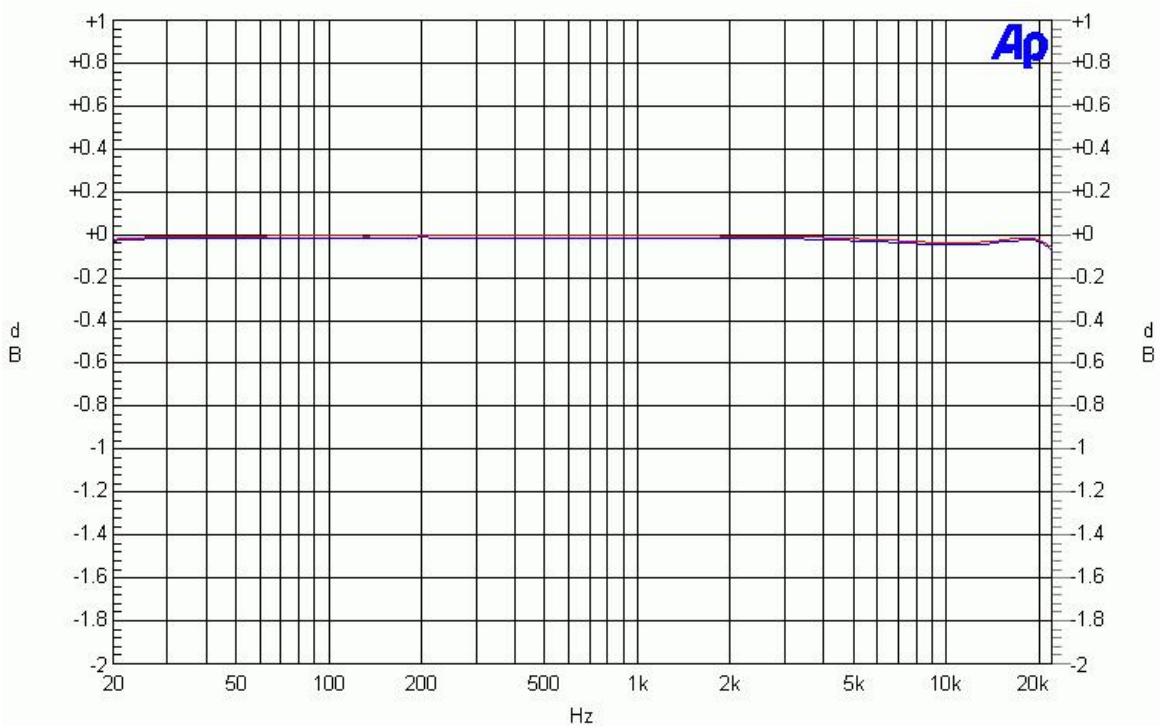
Further Information

power consumption:	2.2 W (typical)
connector style:	XLR 3-pin connectors
printed circuit board (PCB) revision for this specifications:	1

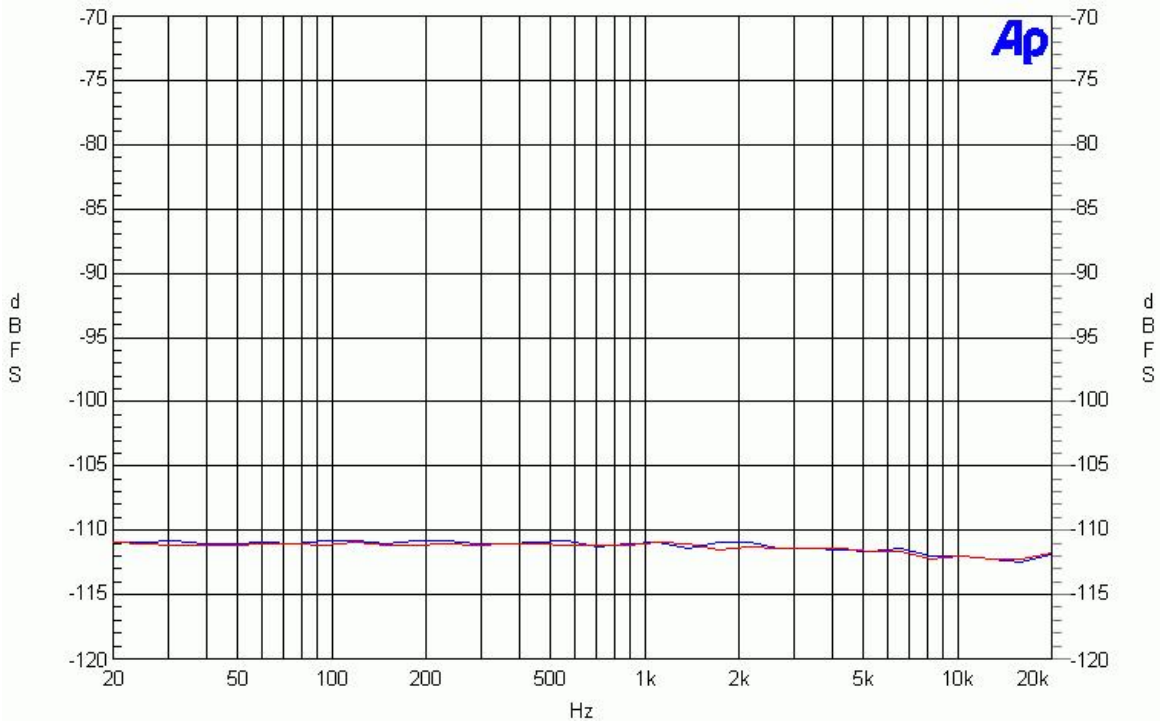
Note

All values are typical values, regarding the factory test limits.

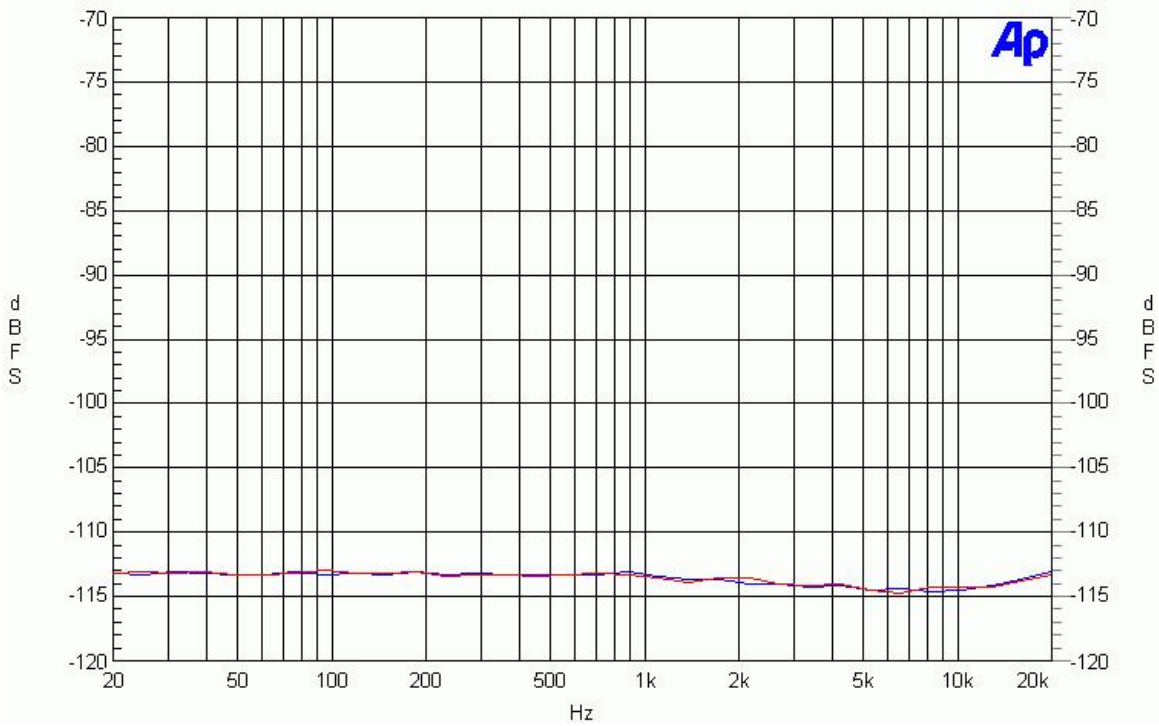
Measurement Plots 52-5213A



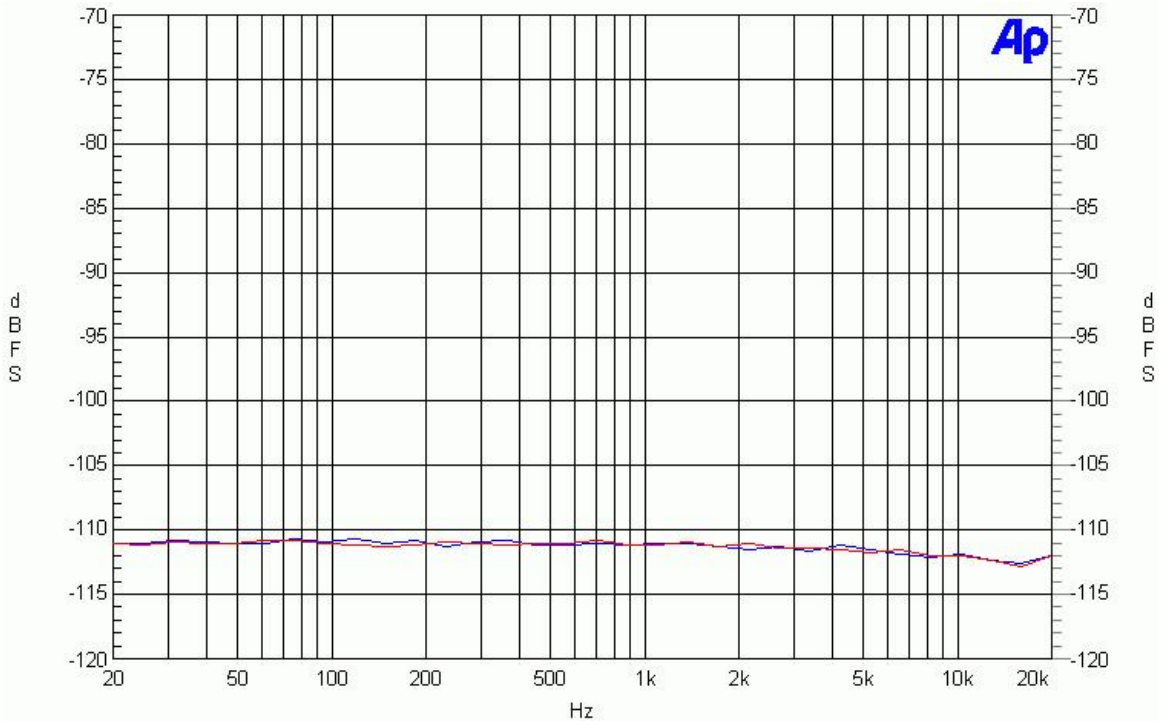
52-5213A ADC Frequency Response



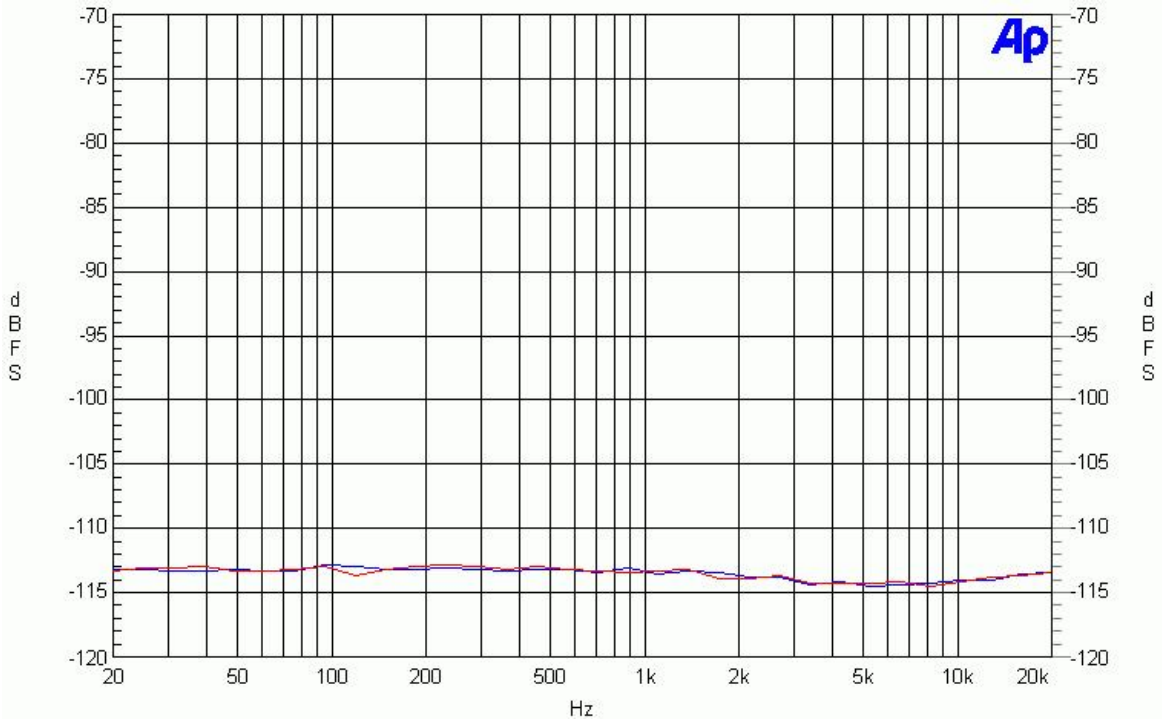
52-5213A ADC THD+N @ -30 dBFS



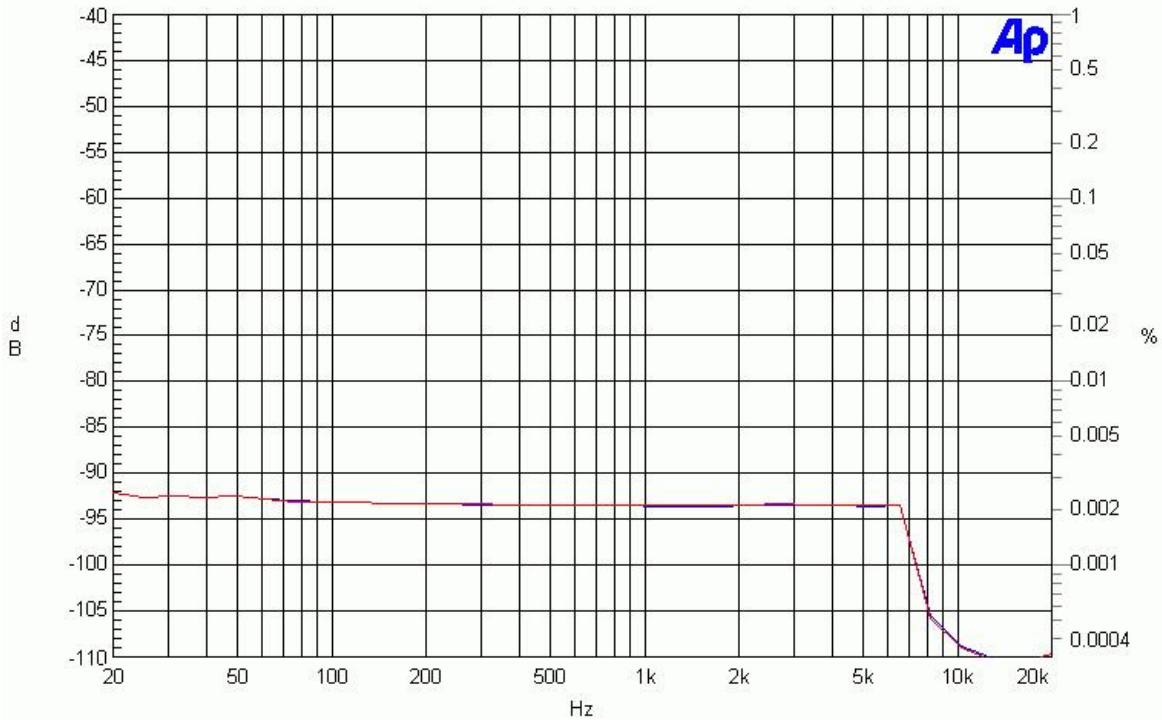
52-5213A ADC THD+N(A) @ -30 dBFS



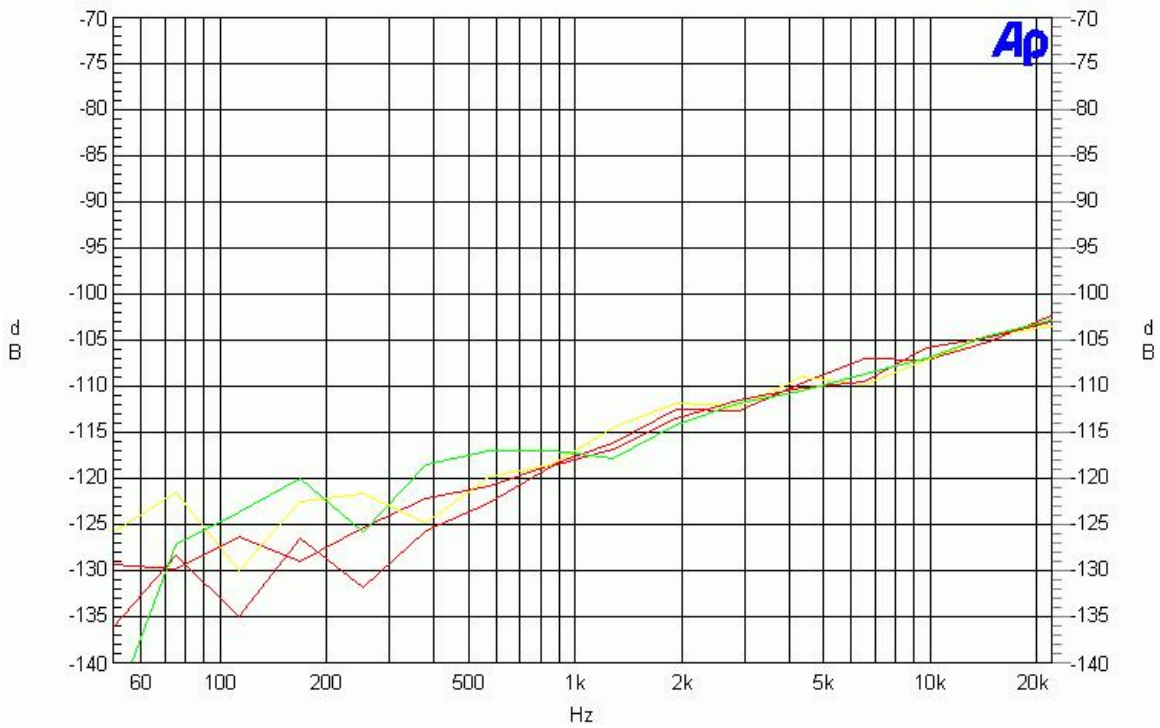
52-5213A ADC THD+N @ +4 dBu



52-5213A ADC THD+N(A) @ +4 dBu

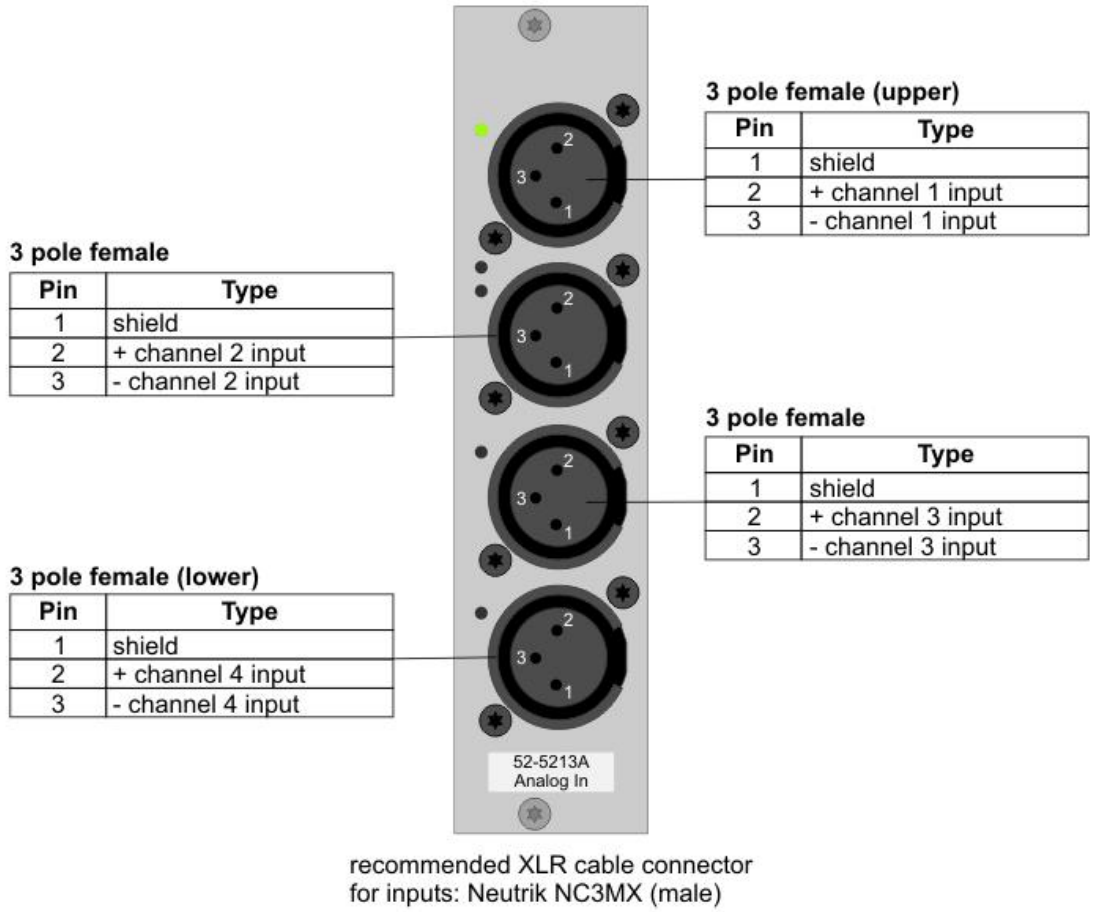


52-5213A ADC THD+N @ +23 dBu



52-5213A ADC Cross-Talk

Pin Assignment



Pin out for the 52-5213 Module.

52-5220A - MB/CR/XD 4 Ch. Line Out, 18dBu

Technical Specifications

D/A Converter

max. output level (phones, single ended):	18 dBu (balanced)
output impedance:	approx. 25 Ohm
minimum load (outputs short circuit protected):	600 Ohm
frequency response:	< 0.1 dB
THD+N:	< -106 dBFS (-30 dBFS, -15 dBu test signal level), (< -91 dBu)
	< -103 dBFS (-9 dBFS, +6 dBu test signal level), (< -88 dBu)
	< -90 dBFS (-1 dBFS, +14 dBu test signal level), (< -75 dBu)
crosstalk:	< -110 dB
dynamic range:	109 dB (A-weighted, 0 dBFS = +15 dBu)
DC offset voltage:	< 30 mV
common mode rejection (output impedance):	> 60 dB
common mode rejection (output voltage):	> 40 dB
converter technology:	24 bit, oversampling sigma-delta

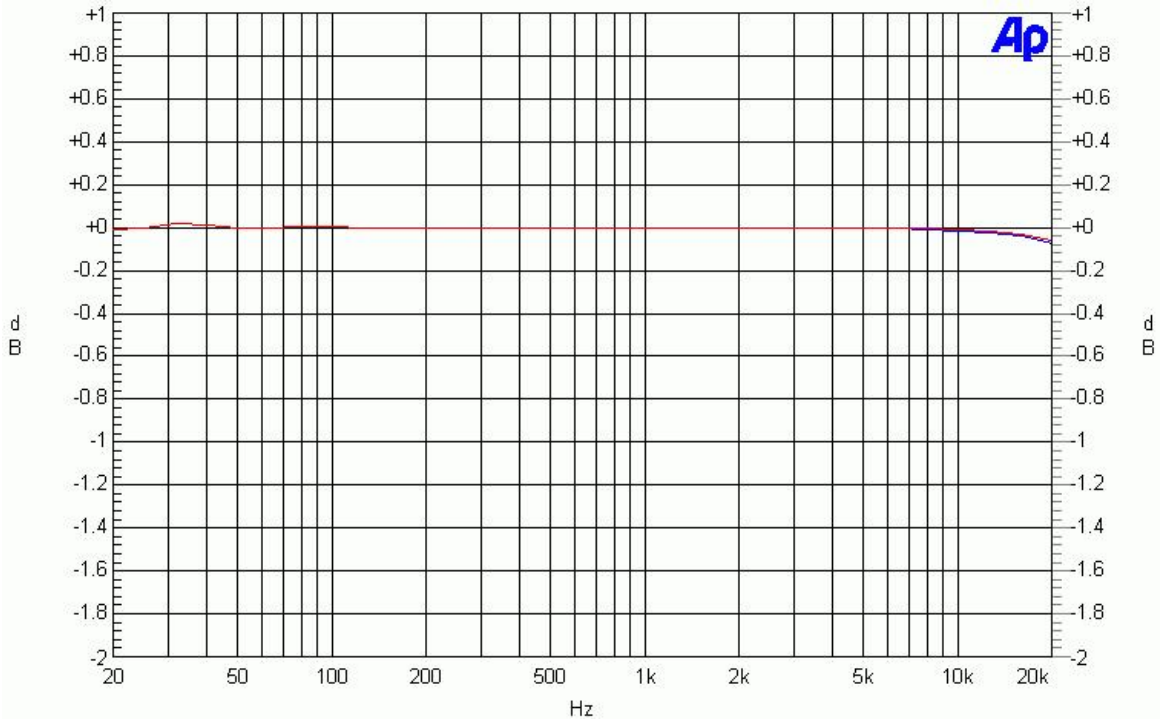
Further Information

power consumption:	2.0 W (typical)
connector style:	XLR 3-pin connectors
printed circuit board (PCB) revision for this specifications:	1

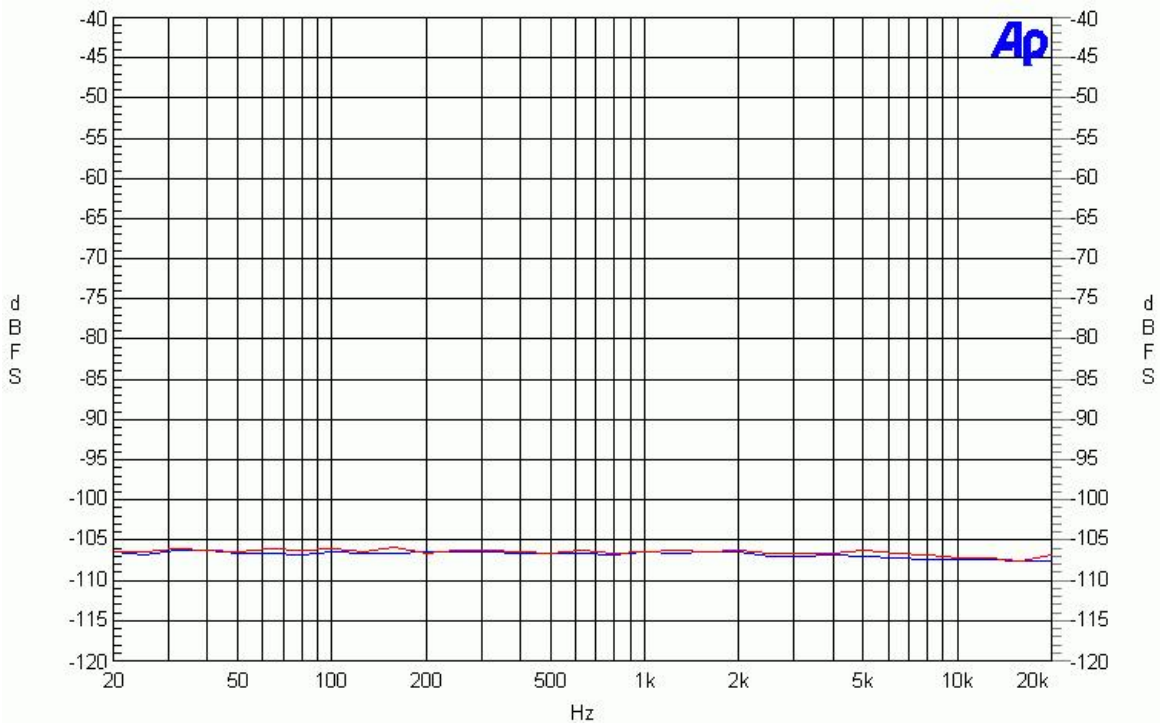
Note

All values are typical values, regarding the factory test limits.

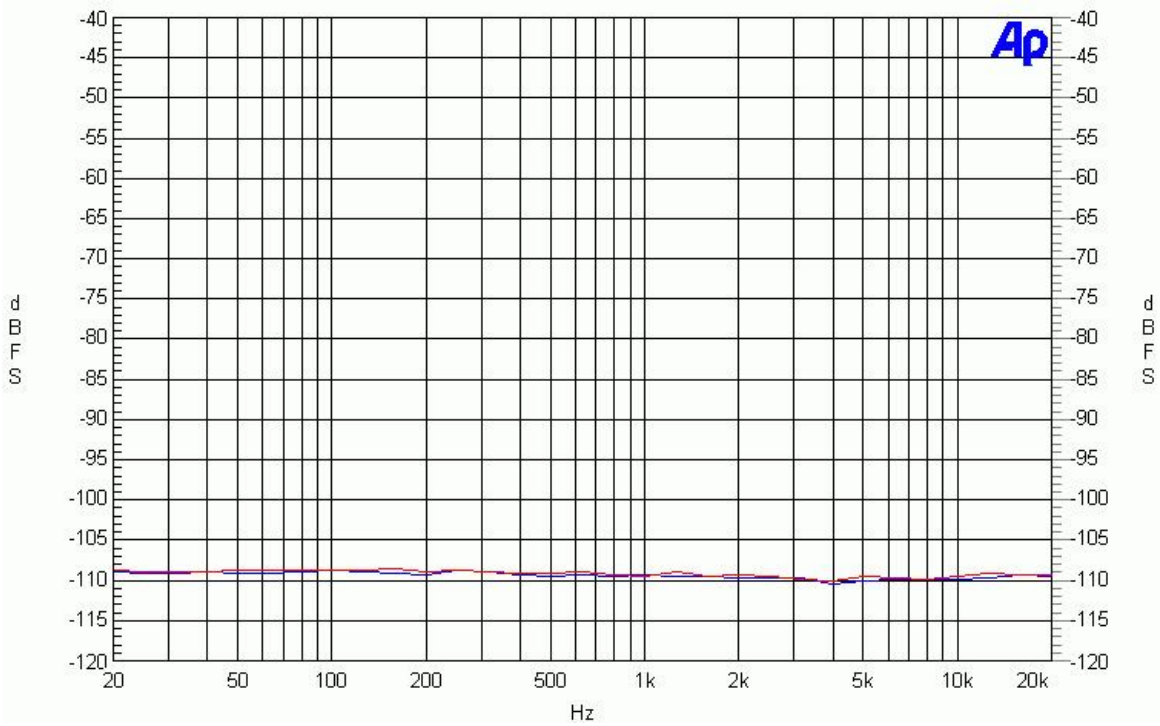
Measurement Plots 52-5220A



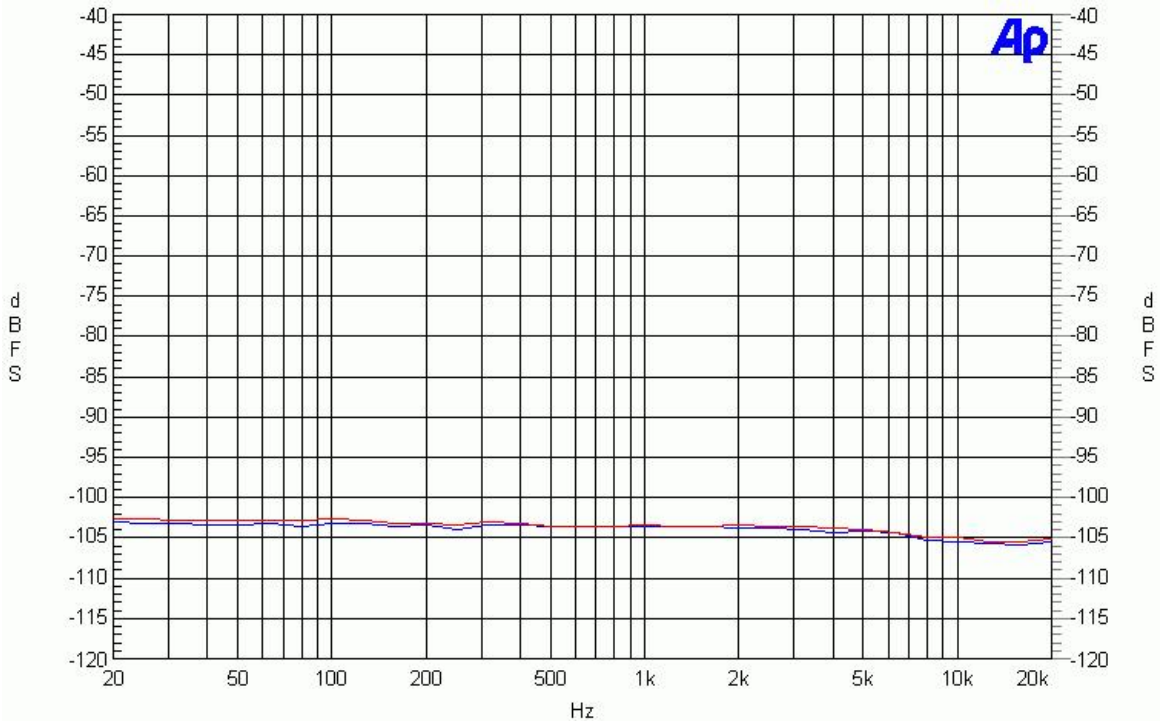
52-5220A DAC Frequency Response



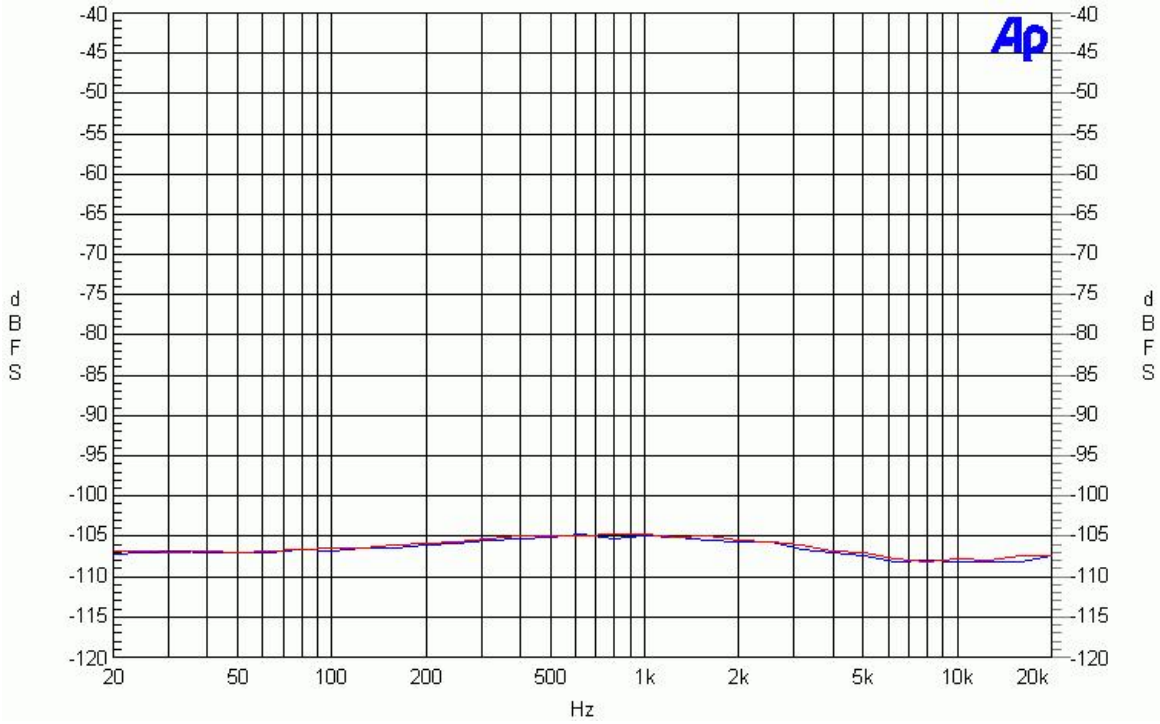
52-5220A DAC THD+N @ -30 dBFS



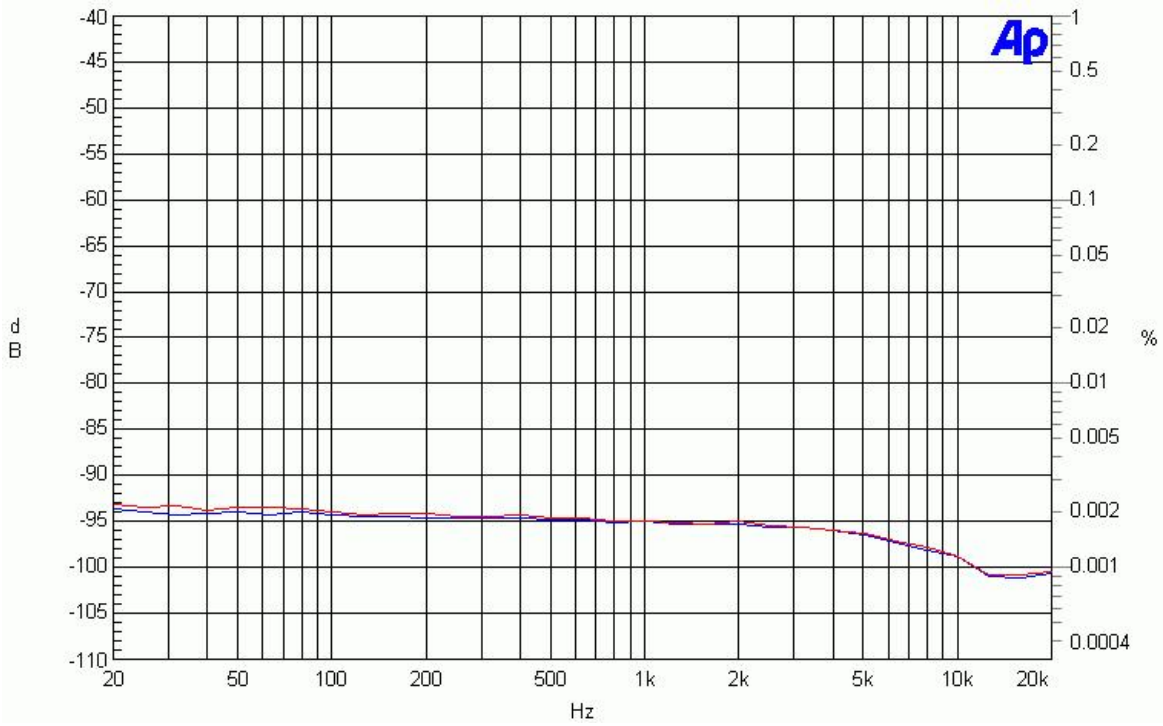
52-5220A DAC THD+N(A) @ -30 dBFS



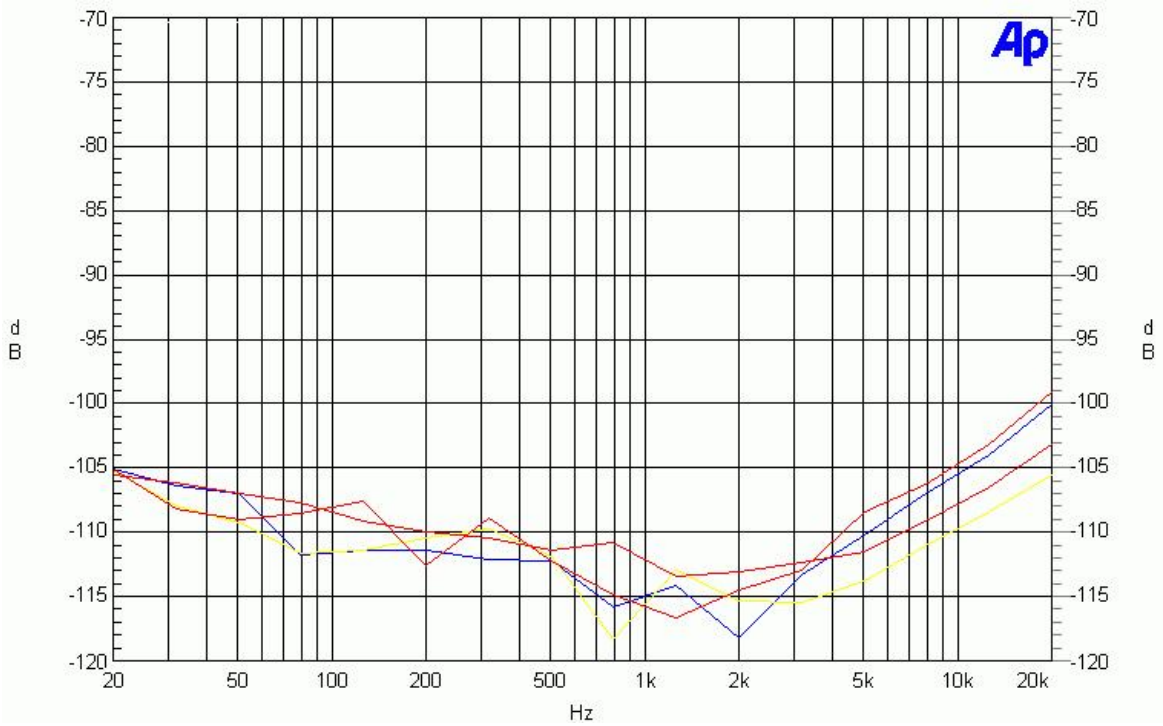
52-5220A DAC THD+N @ +6 dBu



52-5220A DAC THD+N(A) @ +6 dBu

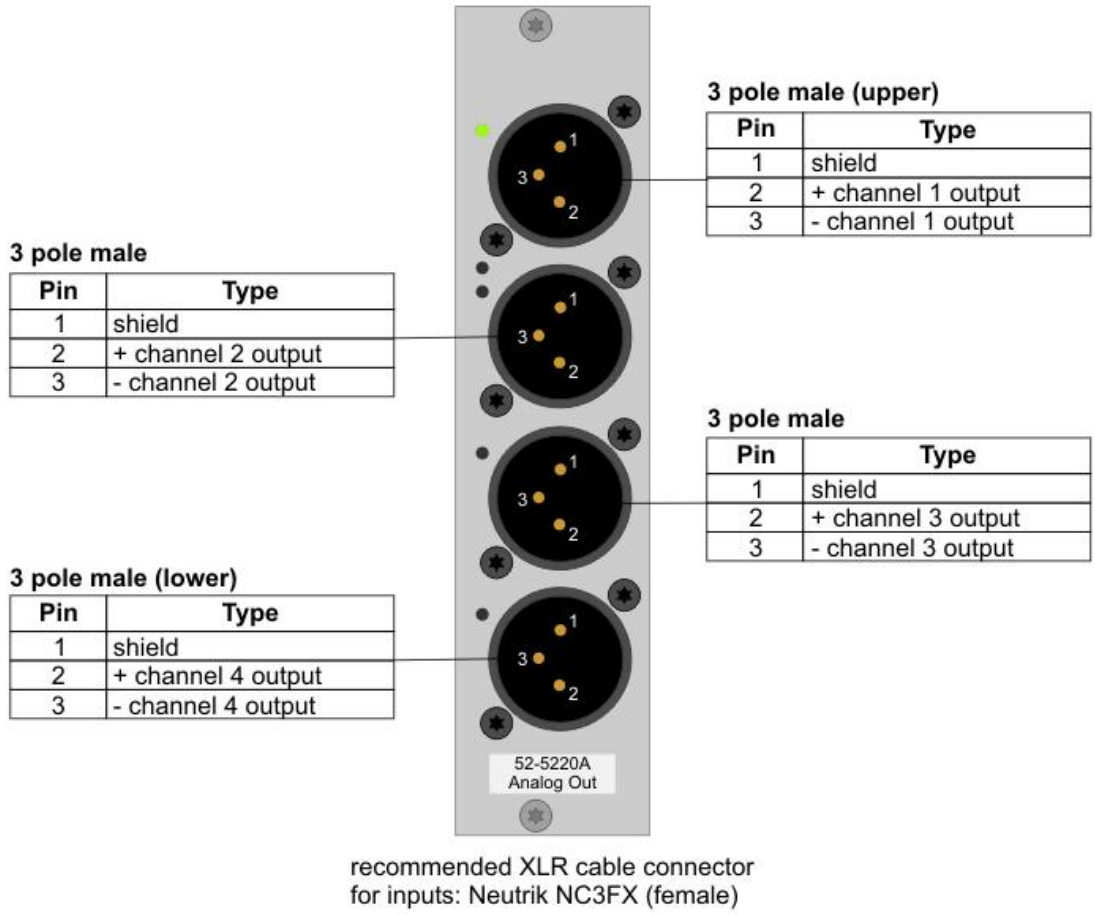


52-5220A DAC THD+N @ +14 dBu



52-5220A DAC Cross-Talk

Pin Assignment



Pin out for the 52-5220 Module.

52-5223A - MB/CR/XD 4 Ch. Line Out, 24dBu

Technical Specifications

D/A Converter

max. output level (phones, single ended):	24 dBu (balanced)
output impedance:	approx. 25 Ohm
minimum load (outputs short circuit protected):	600 Ohm
frequency response:	< 0.1 dB
THD+N:	< -109 dBFS (-30 dBFS, -6 dBu test signal level), (< -85 dBu)
	< -100 dBFS (-20 dBFS, +4 dBu test signal level), (< -76 dBu)
	< -85 dBFS (-1 dBFS, +23 dBu test signal level), (< -61 dBu)
crosstalk:	< -105 dB
dynamic range:	112 dB (A-weighted, 0dBFS = +24 dBu)
DC offset voltage:	< 30 mV
common mode rejection (output impedance):	> 60 dB
common mode rejection (output voltage):	> 40 dB
converter technology:	24 bit, oversampling sigma-delta

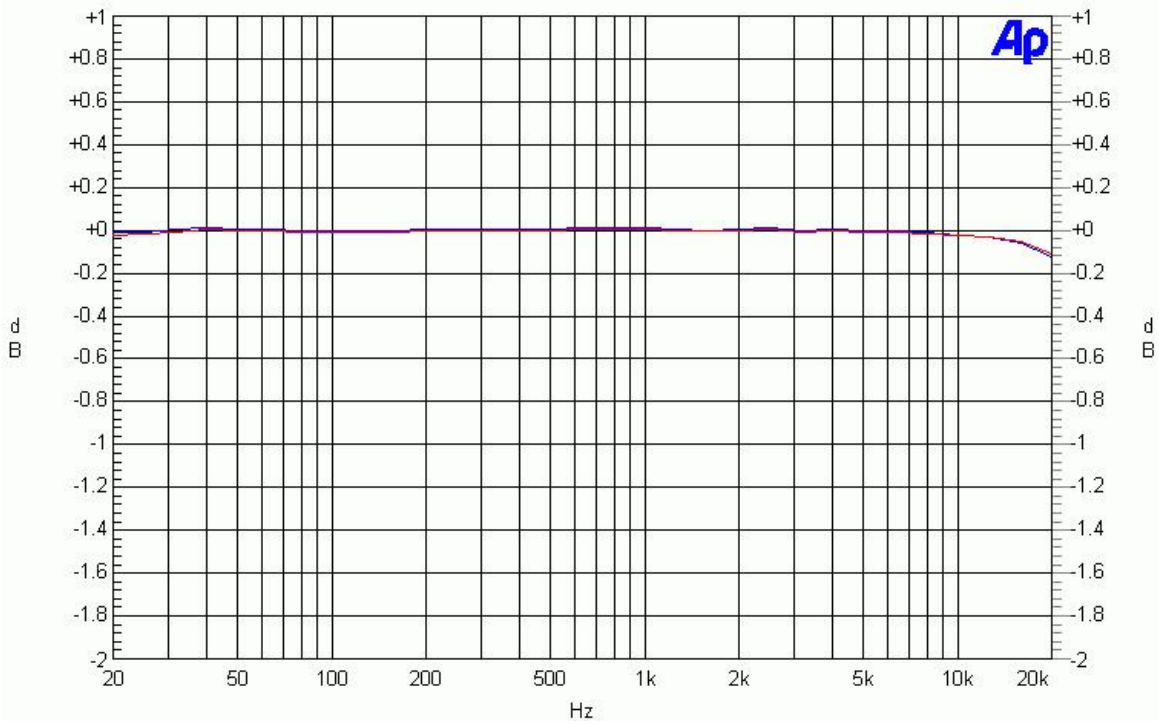
Further Information

power consumption:	2.6 W (typical)
connector style:	XLR 3-pin connectors
printed circuit board (PCB) revision for this specifications:	1

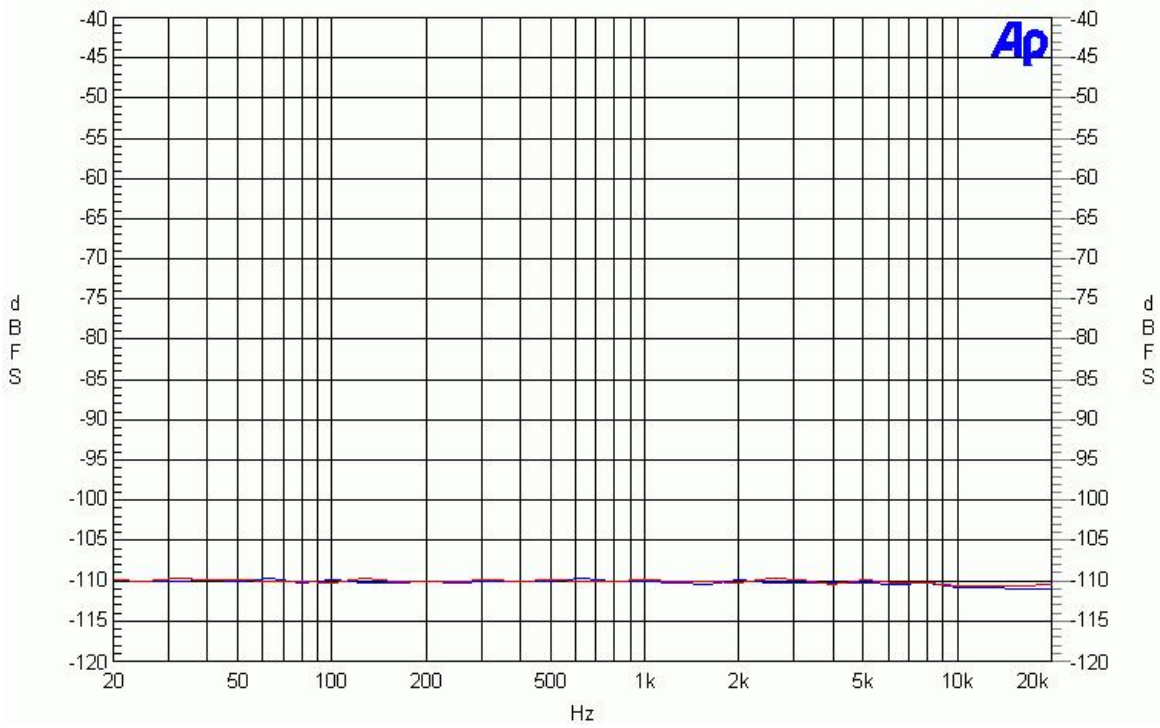
Note

All values are typical values, regarding the factory test limits.

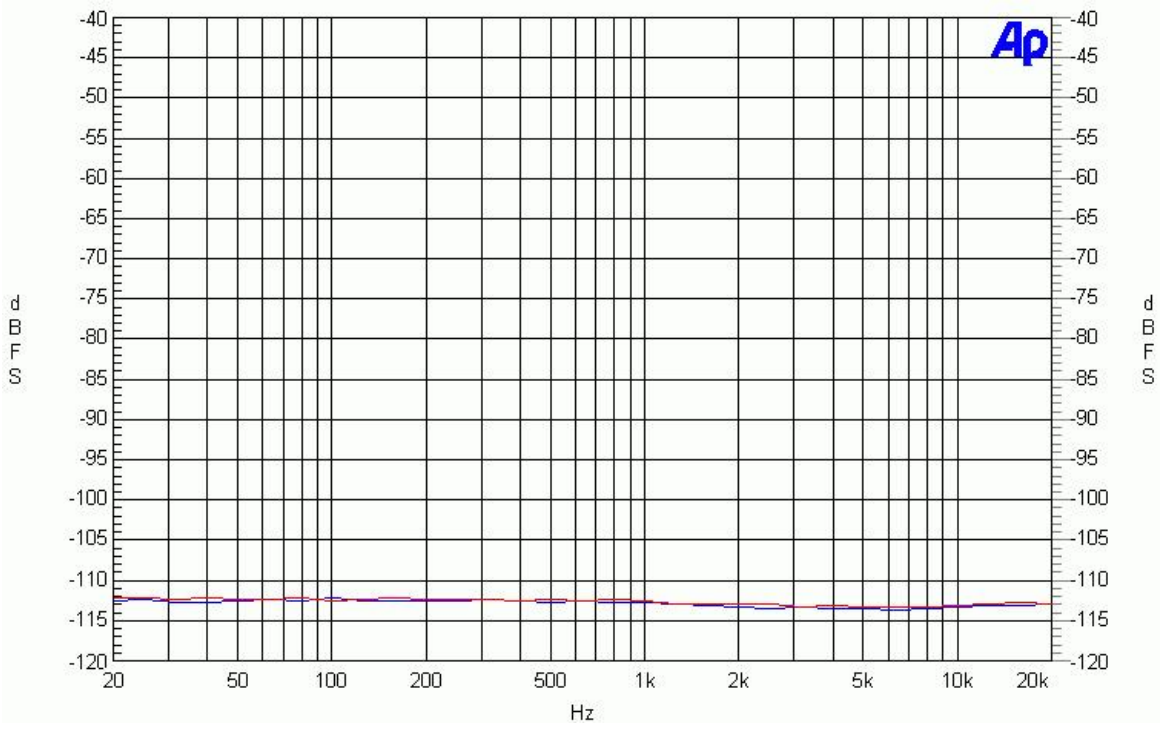
Measurement Plots 52-5223A



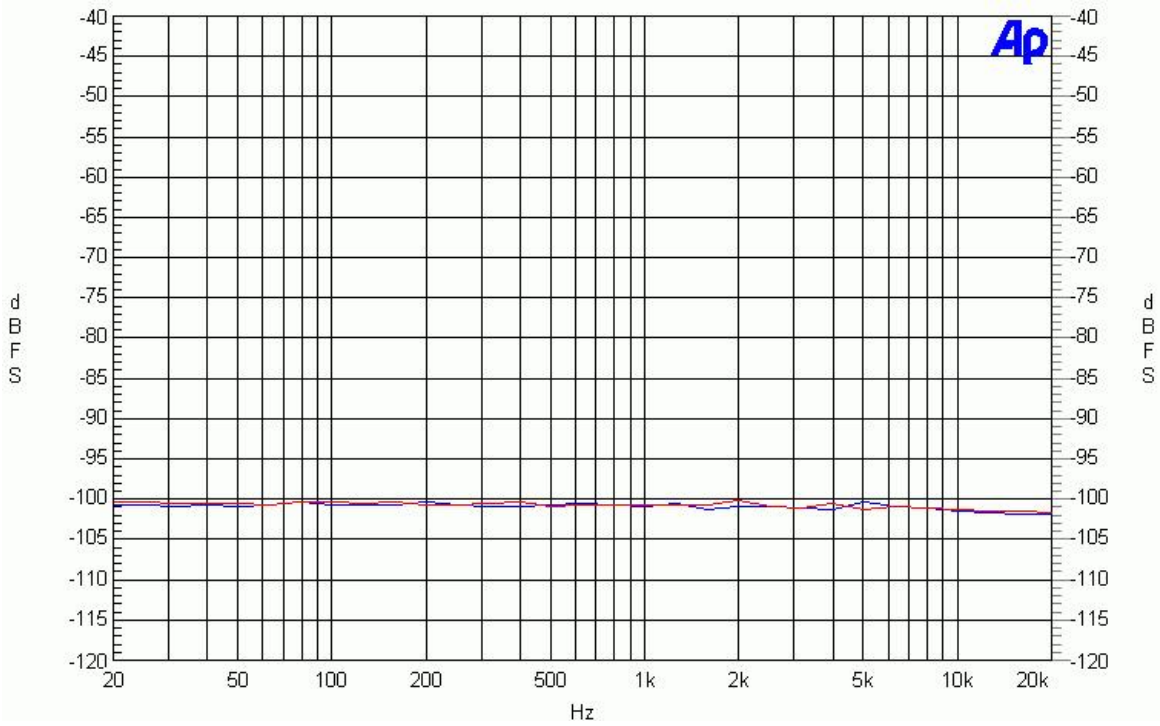
52-5223A DAC Frequency Response



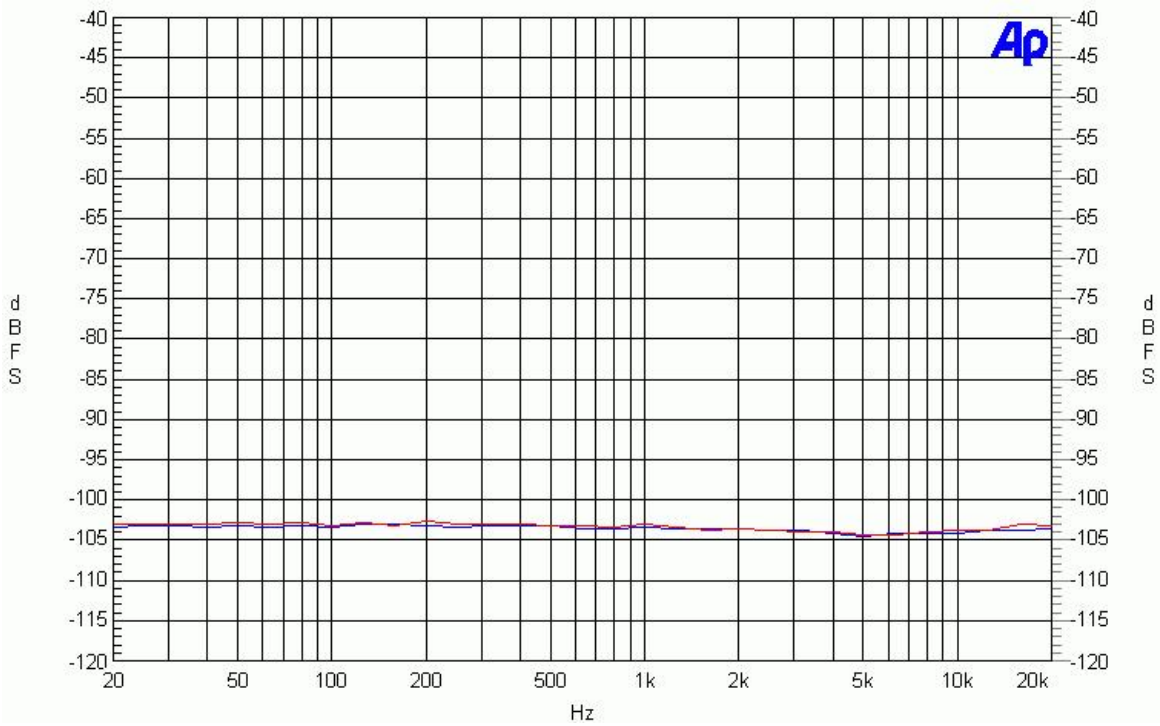
52-5223A DAC THD+N @ -30 dBFS



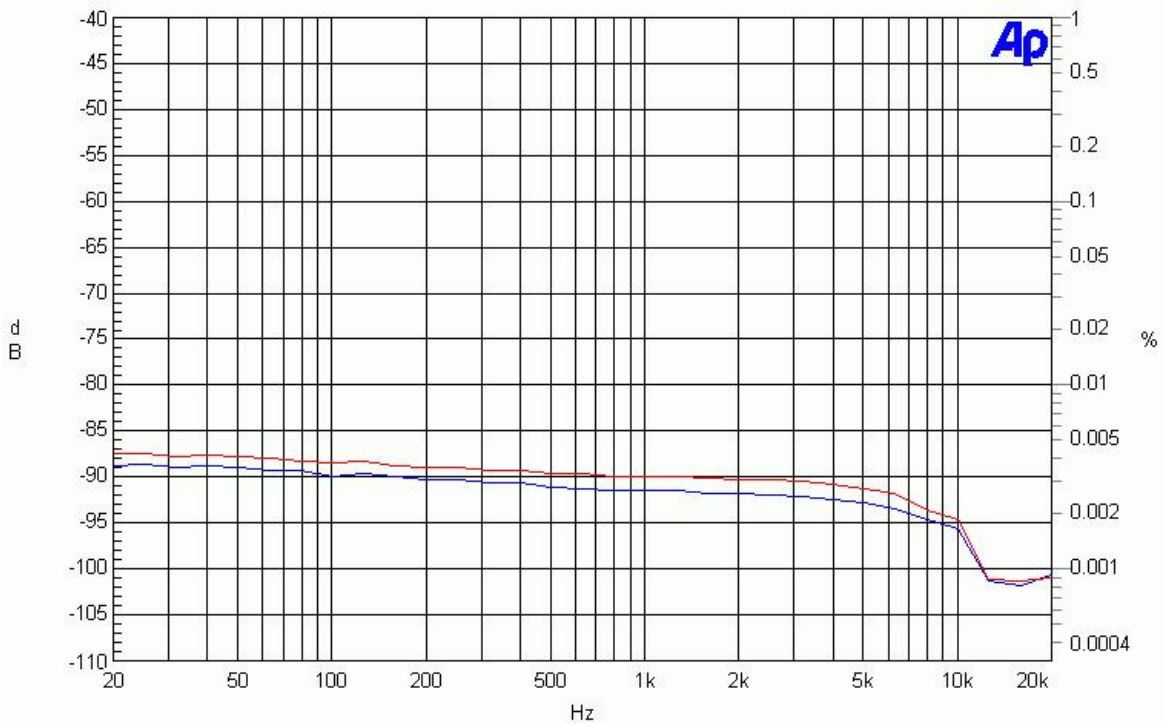
52-5223A DAC THD+N(A) @ -30 dBFS



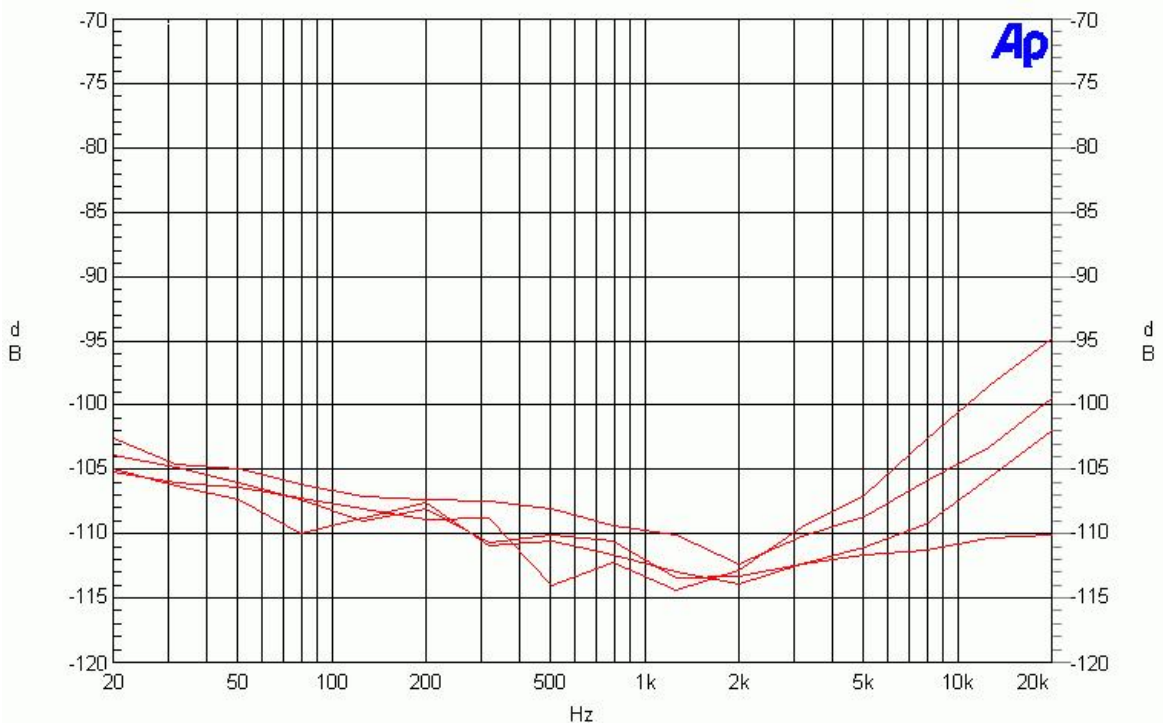
52-5223A DAC THD+N @ +4 dBu



52-5223A DAC THD+N(A) @ +4 dBu

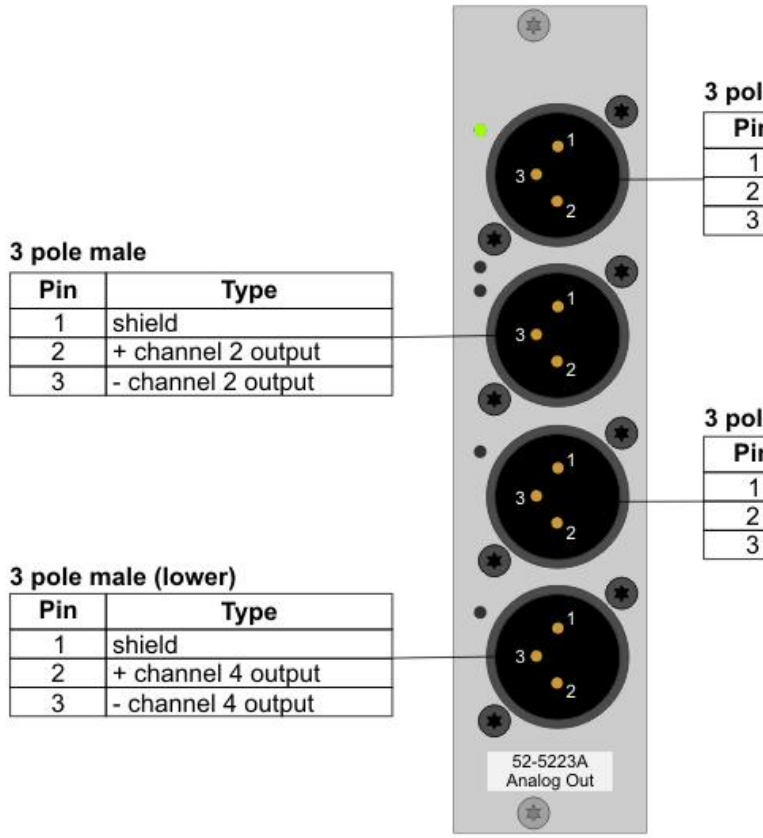


52-5223A DAC THD+N @ -1 dBFS



52-5223A DAC Cross-Talk

Pin Assignment



3 pole male (upper)

Pin	Type
1	shield
2	+ channel 1 output
3	- channel 1 output

3 pole male

Pin	Type
1	shield
2	+ channel 2 output
3	- channel 2 output

3 pole male

Pin	Type
1	shield
2	+ channel 3 output
3	- channel 3 output

3 pole male (lower)

Pin	Type
1	shield
2	+ channel 4 output
3	- channel 4 output

recommended XLR cable connector
for inputs: Neutrik NC3FX (female)

Pin out for the 52-5223 Module.

52-5230A - MB/CR/XD 2 Mic/Headphone Module

Technical Specifications

A/D Converter

max. input level:	26 dBu (balanced)
input impedance:	approx. 5 kOhm
frequency response:	< 0.1 dB
equivalent input noise	< -129 dBu (A-weighted, 200 source impedance, > +30 dB analog gain)
THD+N:	< -112 dBFS (-30 dBFS, +10 dB analog gain) < -100 dBFS (-1 dBFS, +10 dB analog gain)
crosstalk:	< -123 dB (1kHz)
phantom power 48V:	switchable per input channel, unloaded input: 48V +/- 10%
dynamic range:	112 dB (A-weighted, +10 dB analog gain)
common mode rejection:	> 60 dB
converter technology:	24 bit, oversampling sigma-delta

D/A Converter

max. output level (headphones, single ended):	15 dBu
output impedance:	approx. 65 Ohm
load impedance (outputs short circuit protected):	> 80 Ohm
frequency response:	< 0.05 dB
THD+N:	< -106 dBFS (-30 dBFS) < -103 dBFS (-9 dBFS, +6 dBu) < -95 dBFS (-1 dBFS, +14dBu)
crosstalk:	< -110 dB (1 kHz)

D/A Converter

dynamic range:	110dB (A-weighted)
DC offset voltage:	< 10 mV
converter technology:	24 bit, oversampling sigma-delta

Further Information

power consumption:	3.0 W (typical)
connector style:	XLR 3-pin connectors, combined XLR 3-pin and jack sockets
printed circuit board (PCB) revision for this specifications:	1

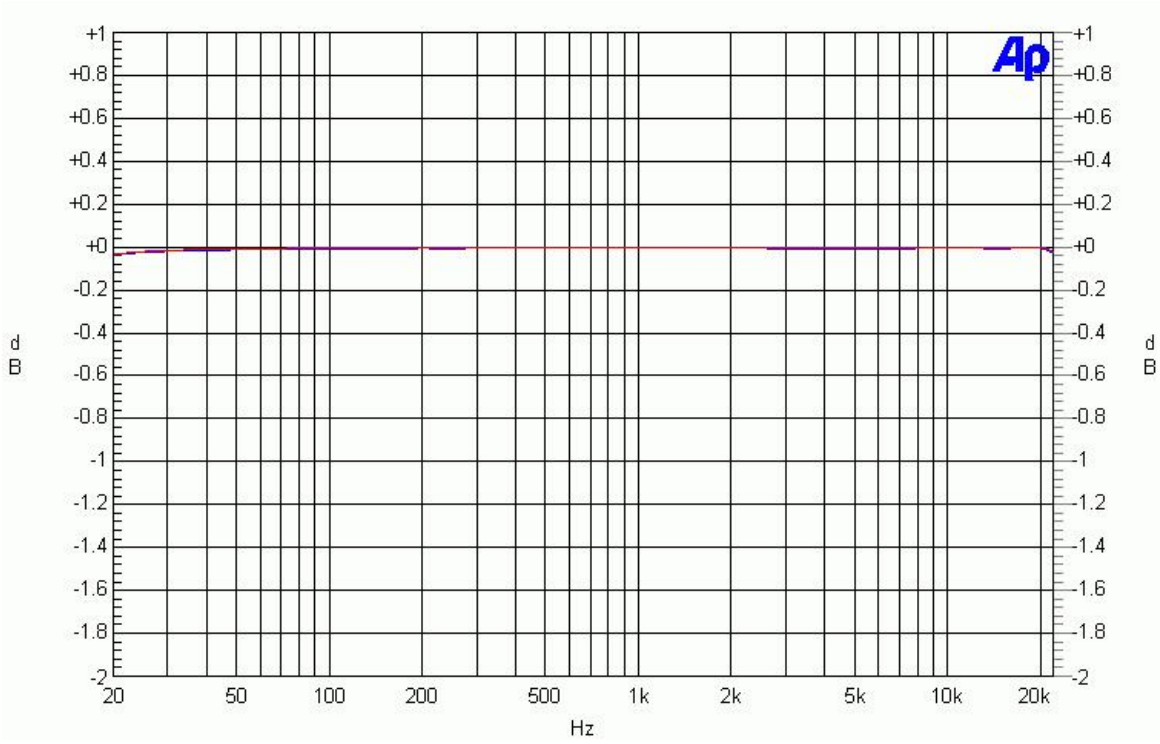
Note

All values are typical values, regarding the factory test limits.

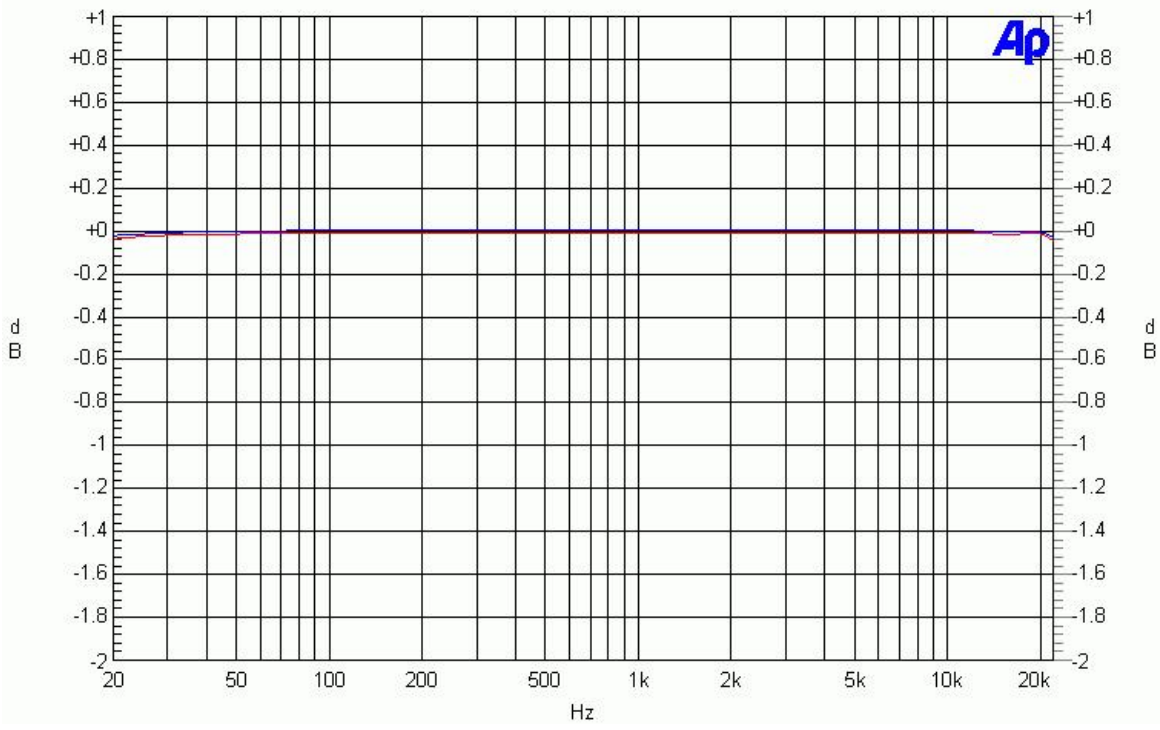
Warning

The wiring of microphone inputs of DHD microphone input modules is not designed to support operation with parallel external phantom power. Using it might result in damages of pre-amplifier or phantom power generator.

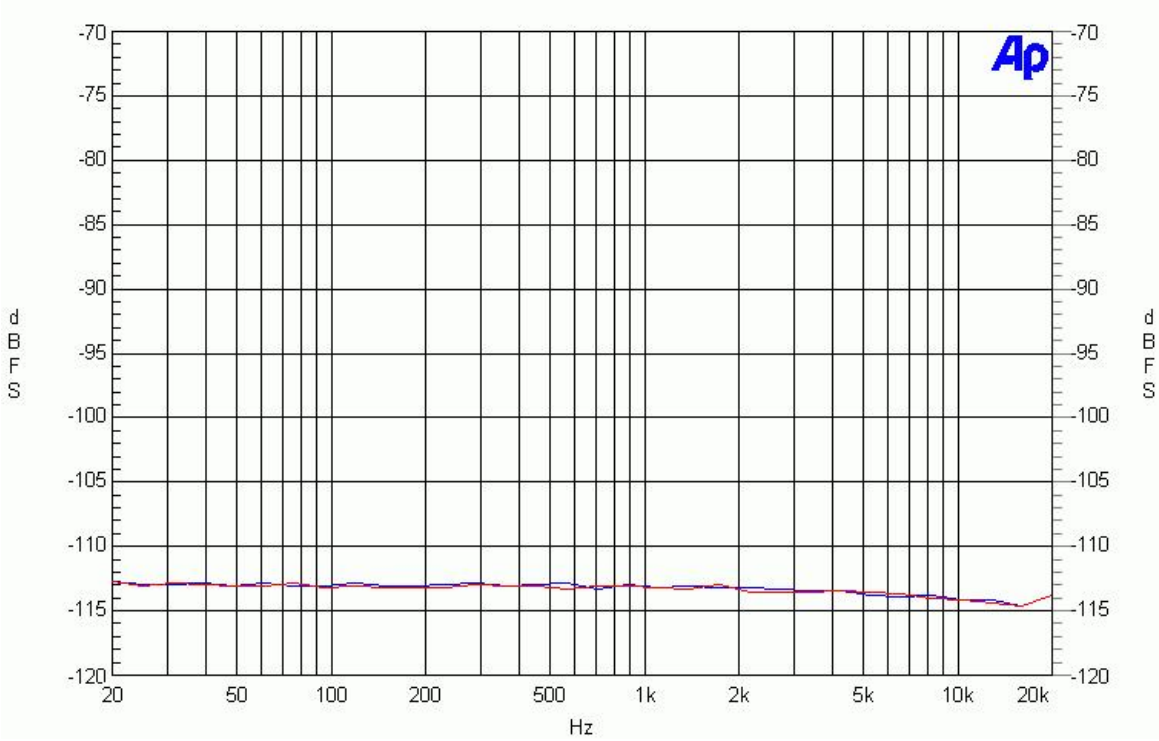
Measurement Plots 52-5230A Inputs



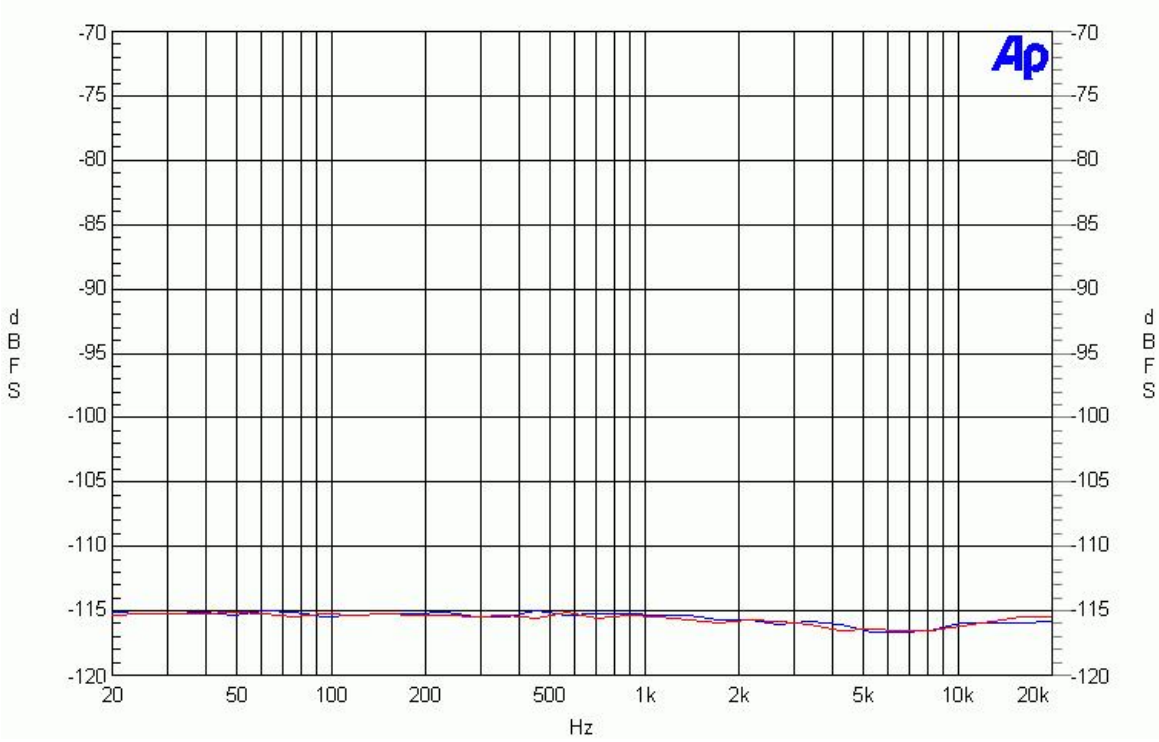
52-5230A Frequency Response, Pad OFF



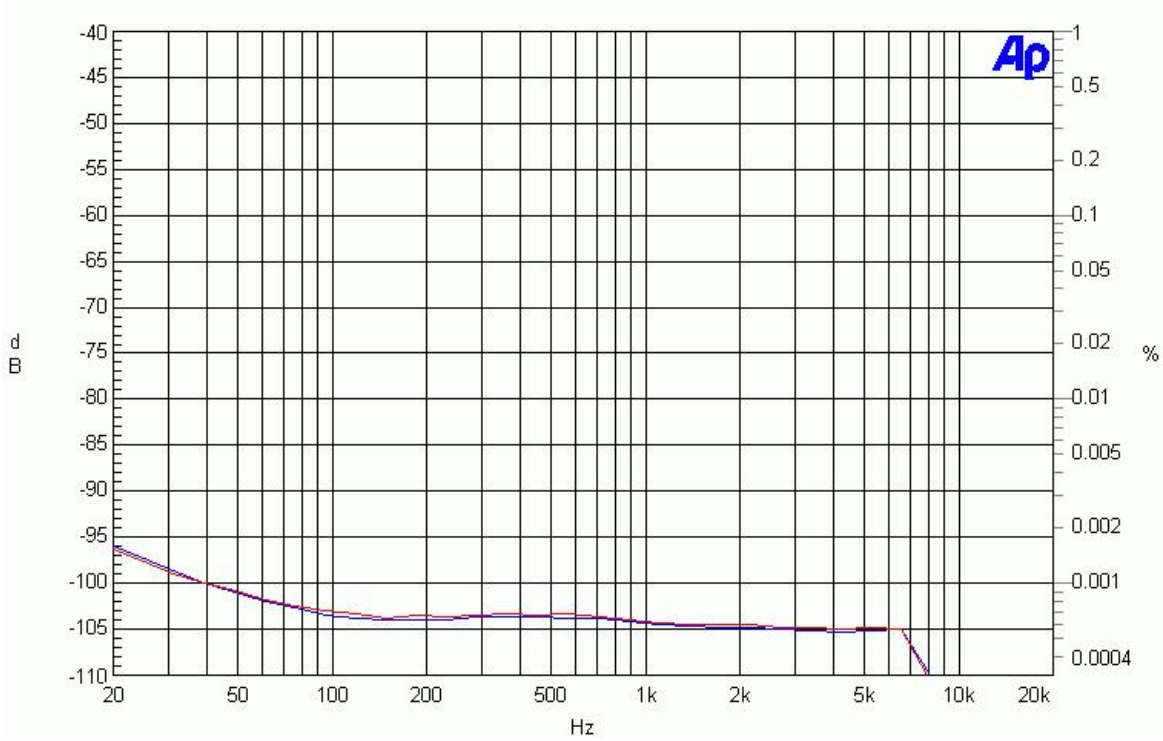
52-5230A Frequency Response, Pad ON



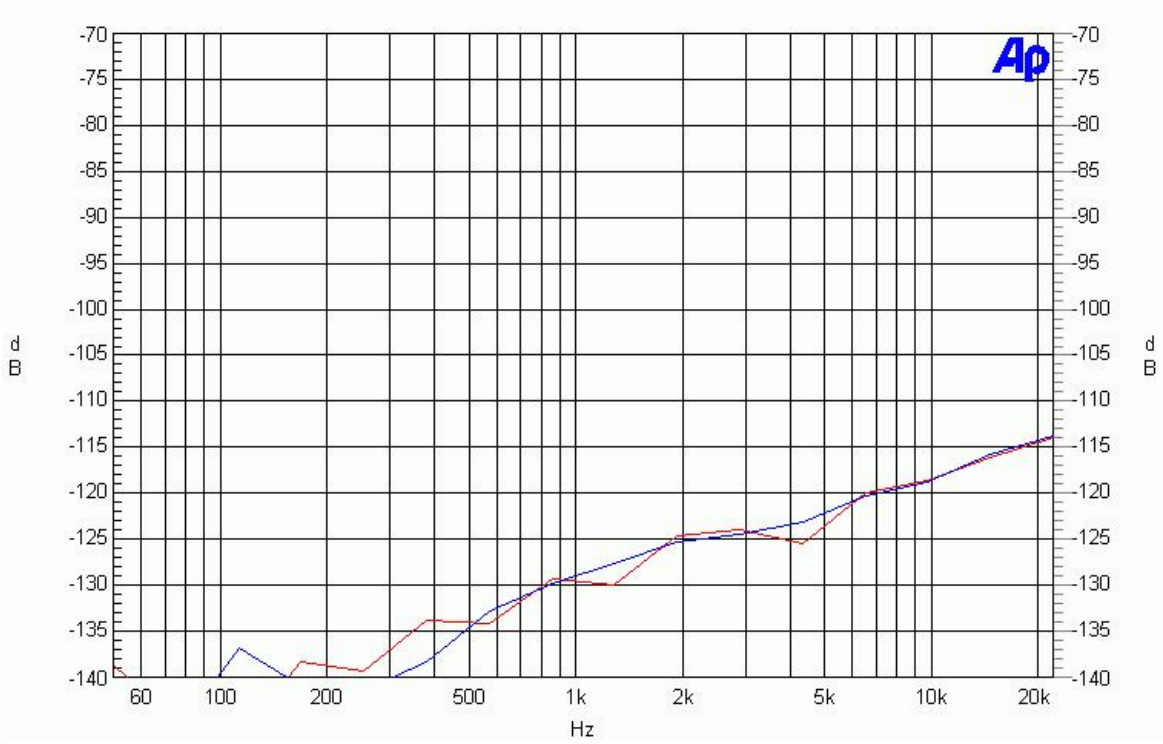
52-5230A THD+N @ -30 dBFS



52-5230A THD+N(A) @ -30 dBFS

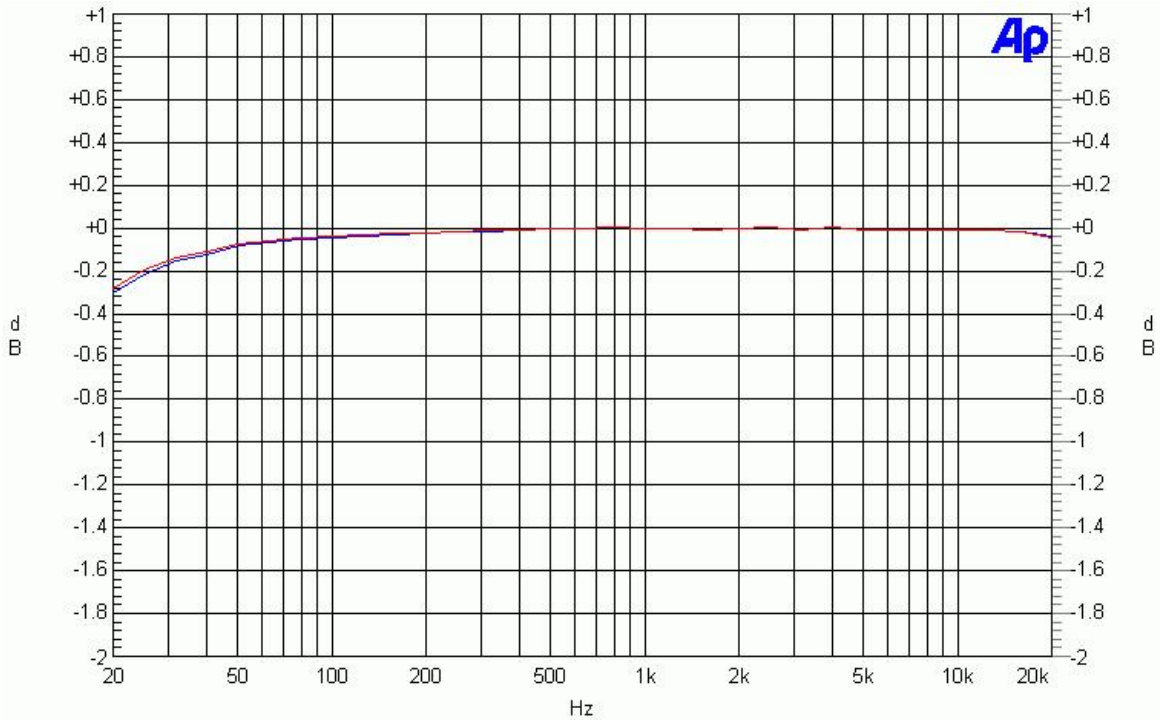


52-5230A THD+N @ +14 dBu

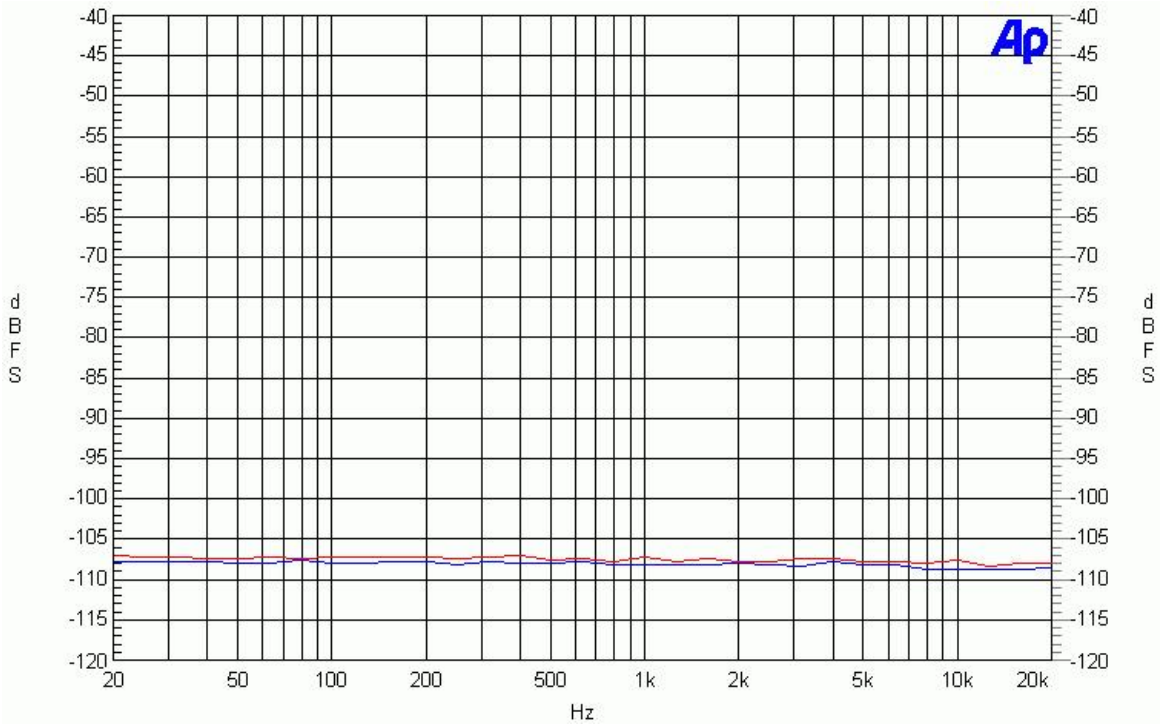


52-5230A Cross-Talk

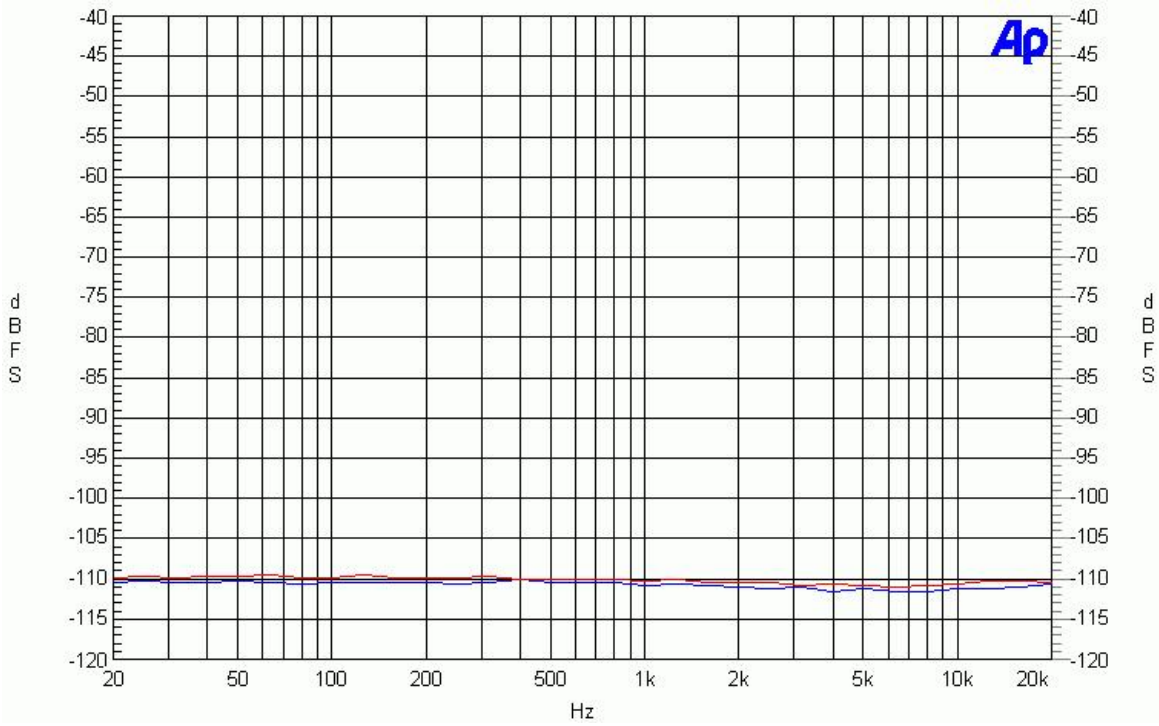
Measurement Plots 52-5230A Outputs



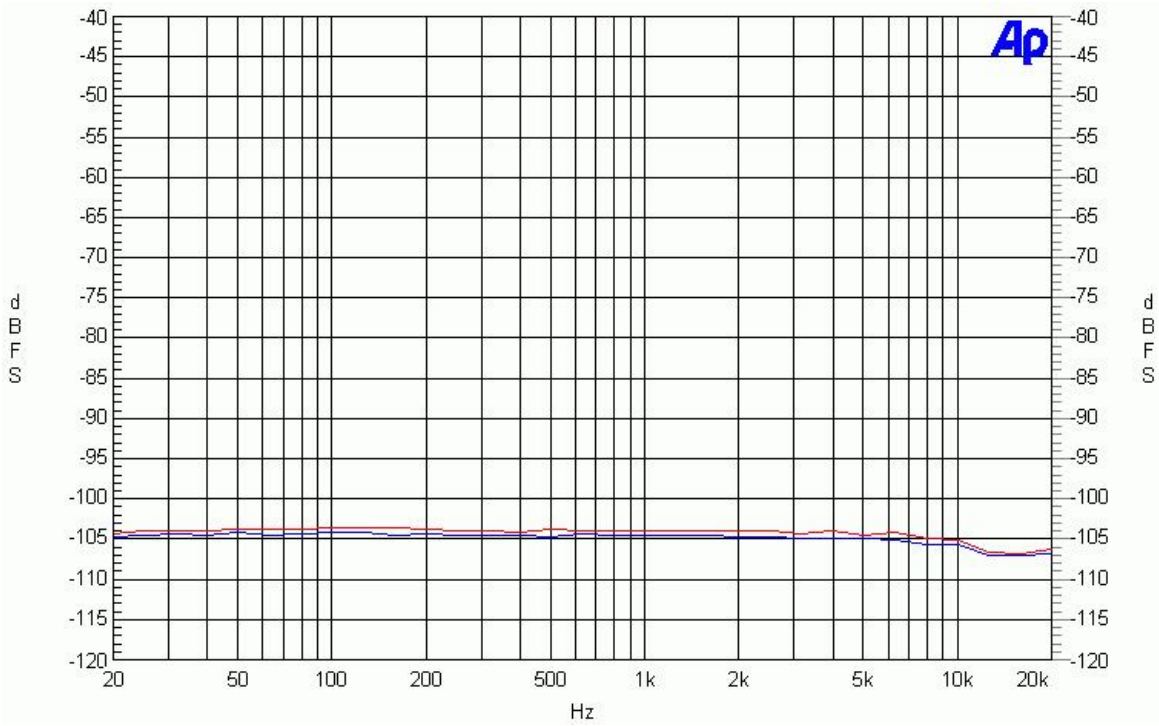
52-5230A DAC Frequency Response



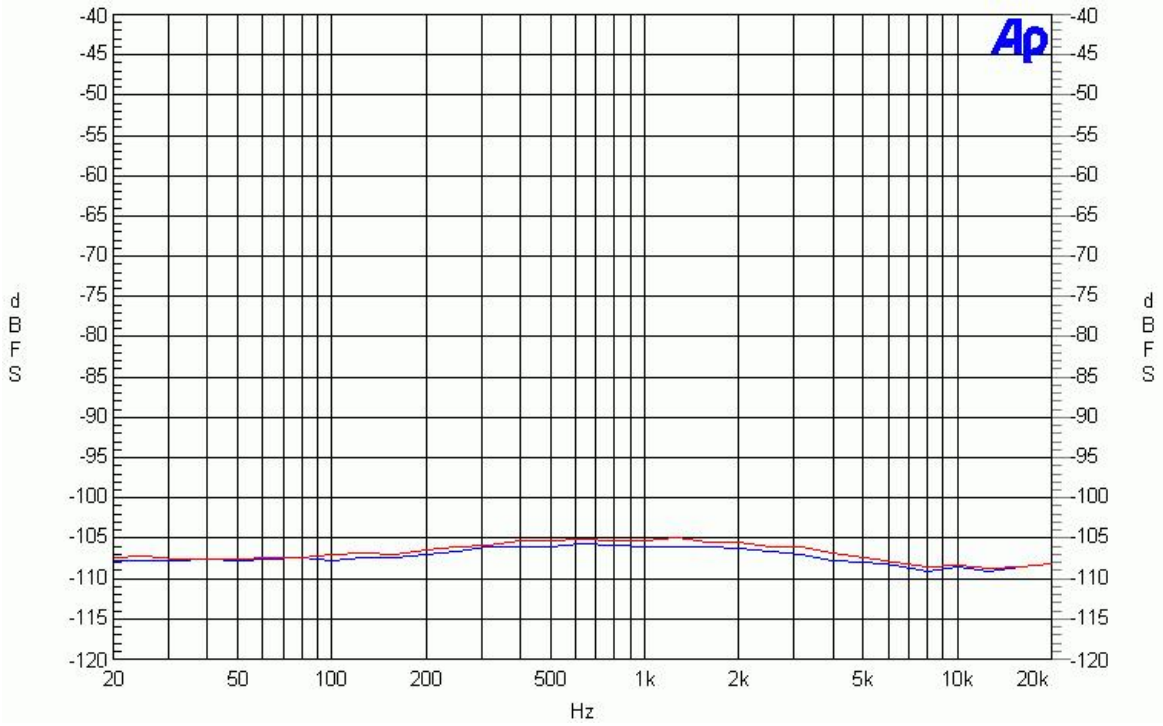
52-5230A DAC THD+N @ -30 dBFS



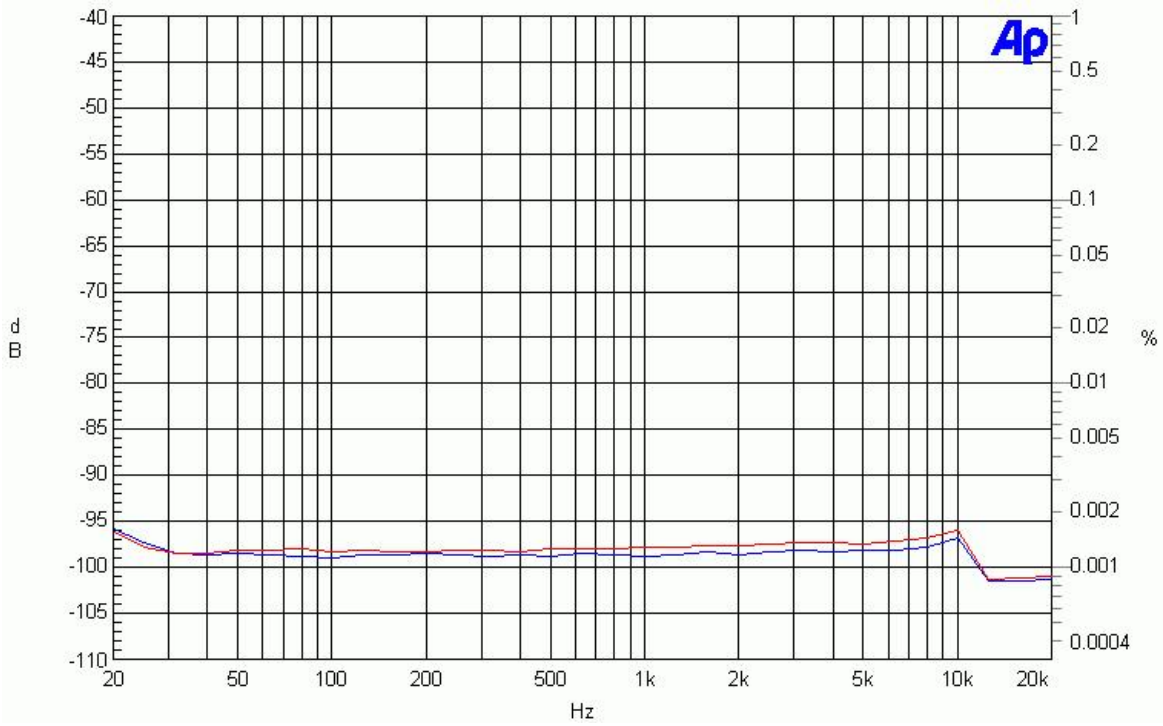
52-5230A DAC THD+N(A) @ -30 dBFS



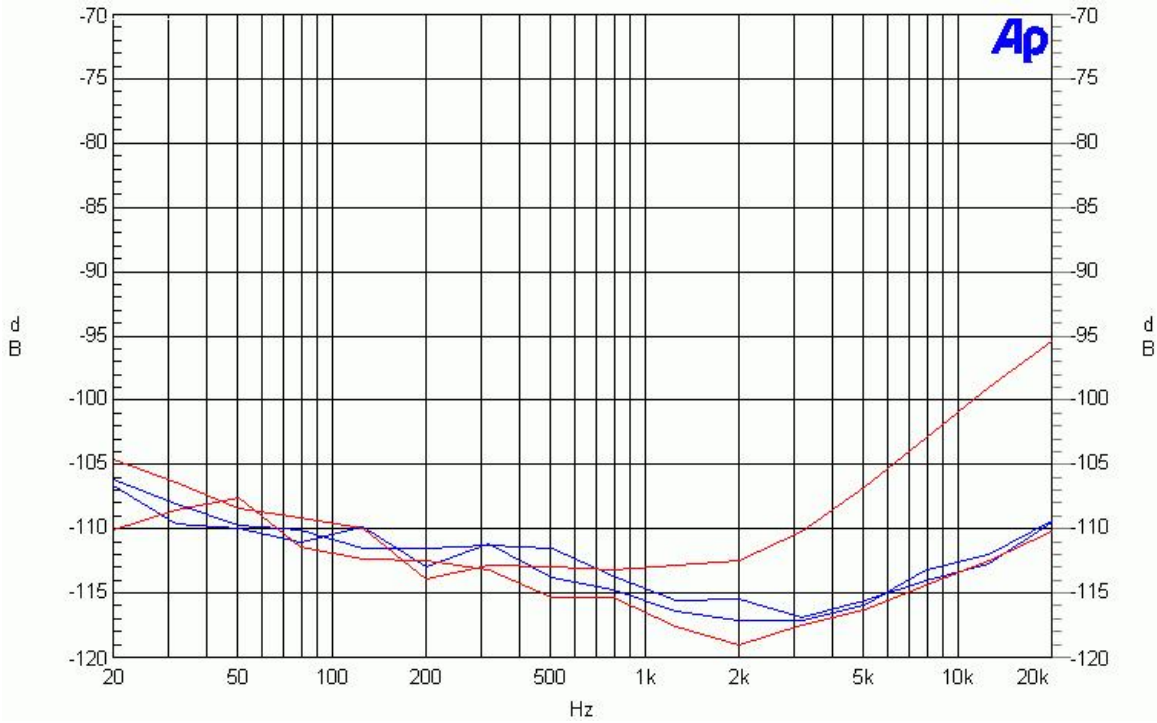
52-5230A DAC THD+N @ +6 dBu



52-5230A DAC THD+N(A) @ +6 dBu



52-5230A DAC THD+N @ +14 dBu, 300Ohm



52-5230A DAC Cross-Talk

Log File Example

After manufacturing all inputs and outputs of every I/O card are measured. Hence, we can make sure that every module, leaving the production hall, is working correctly. During this process a log file is written. This file is saved by DHD for maintenance purposes.

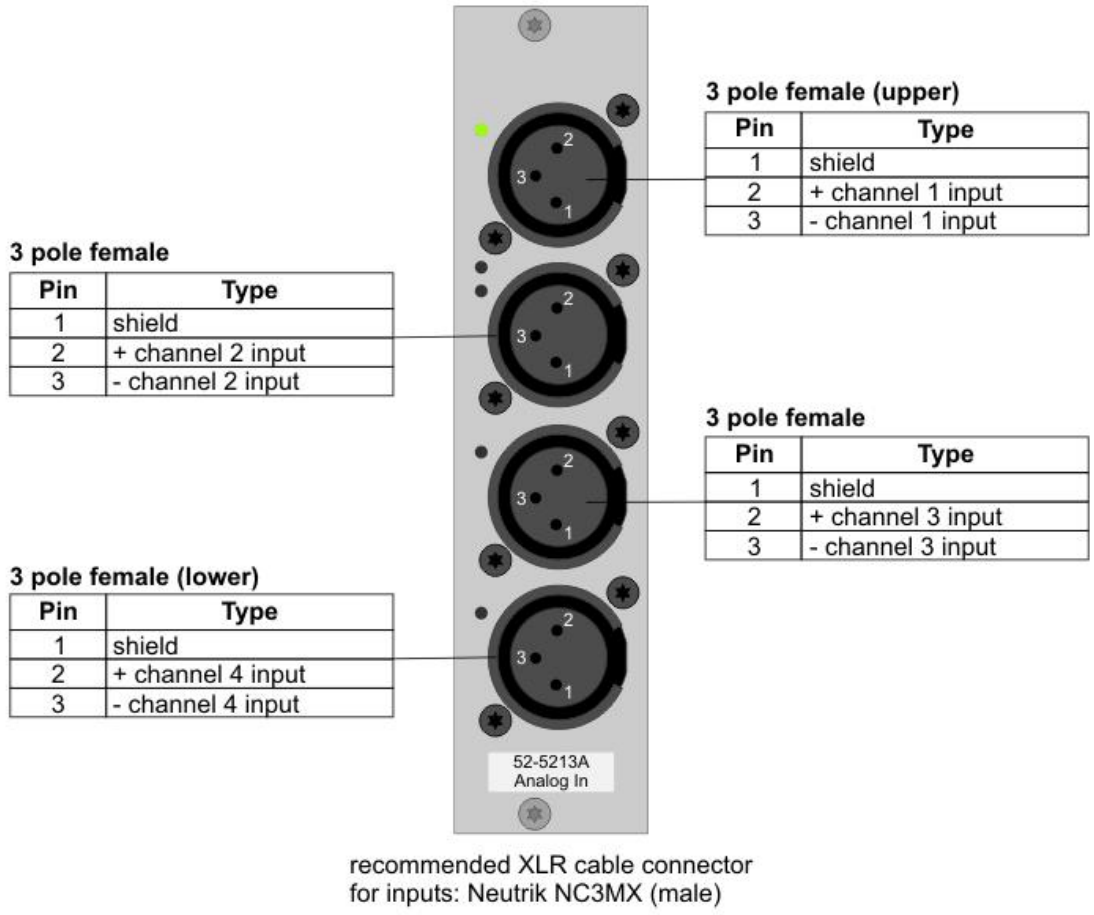
In the following you can find a log file example of an 52-5230 module:

```
*** Factory Test z52-52301 ***

=== 1.2V power supply ===
VCC1V2=1.235 V
=== 2.5V power supply ===
VCC2V5=2.547 V
=== 3.3V power supply ===
VCC3=3.301 V
=== 5V power supply ===
VCC5=5.094 V
=== 48V phantom power ===
V48=49.3 V
=== +10V analog power ===
V10+=10.0 V
=== -10V analog power ===
V10-=-9.8 V

=== DAC Level Ch.1-2 ===
Gain(1kHz): L=-2.97 dB,  R=-3.05 dB
Polarity: (+)
total group delay @ 48.0kHz: L=1.18ms,  R=1.18ms (L=56.5,  R=56.5 Samples)
ripple (20Hz..20000Hz) L=0.022 dB, R=0.016 dB
dynamic:  L=95.6 dB,     R=96.7 dB

=== DAC Level Ch.3-4 ===
Gain(1kHz): L=-3.09 dB,  R=-3.18 dB
Polarity: (+)
total group delay @ 48.0kHz: L=1.18ms,  R=1.18ms (L=56.5,  R=56.5 Samples)
ripple (20Hz..20000Hz) L=0.010 dB, R=0.008 dB
dynamic:  L=96.4 dB,     R=97.4 dB

=== Distortion 300 Ohm Load Ch.1-2 ===
Gain(1kHz): L=-4.71 dB,  R=-4.70 dB
ripple (20Hz..20000Hz) L=0.021 dB, R=0.025 dB
```

```
Output Impedance:  L=66.2 Ohm,  R=65.8 Ohm
dynamic:  L=98.7 dB,     R=99.8 dB

=== Distortion 300 Ohm Load Ch.3-4 ===
Gain(1kHz): L=-4.71 dB,  R=-4.70 dB
ripple (20Hz..20000Hz) L=0.022 dB, R=0.028 dB
Output Impedance:  L=66.1 Ohm,  R=65.9 Ohm
dynamic:  L=99.3 dB,     R=100.4 dB

=== DAC Dynamic Ch.1-2 ===
dynamic:  L=112.3 dB,     R=112.8 dB

=== DAC Dynamic Ch.3-4 ===
dynamic:  L=112.3 dB,     R=113.0 dB

=== ADC Level Ch.1-2, Pad on ===
Gain(1kHz): L=-8.13 dB,  R=-8.13 dB
Polarity: (+)
total group delay @ 48.0kHz: L=1.18ms,  R=1.18ms (L=56.5,  R=56.5 Samples)
ripple (20Hz..20000Hz) L=0.031 dB, R=0.035 dB
dynamic:  L=108.8 dB,     R=109.3 dB

=== ADC Level Ch.1-2, Pad off ===
Gain(1kHz): L=3.92 dB,  R=3.93 dB
Polarity: (+)
total group delay @ 48.0kHz: L=1.18ms,  R=1.18ms (L=56.5,  R=56.5 Samples)
ripple (20Hz..20000Hz) L=0.030 dB, R=0.034 dB
dynamic:  L=102.9 dB,     R=102.3 dB

=== ADC Dynamic Ch.1-2 ===
ripple (20Hz..20000Hz) L=0.149 dB, R=0.739 dB
!!! minimum limit violation (amplitude < -0.5 dB))
!!! maximum limit violation (amplitude > -0.1 dB))
dynamic:  L=111.0 dB,     R=111.0 dB
ripple (20Hz..20000Hz) L=0.065 dB, R=0.067 dB
dynamic:  L=111.1 dB,     R=111.1 dB

=== ADC Common Mode Rejection Ch.1-2 ===
worst case CMR (20Hz..15000Hz):  L=72.5 dB, R=64.6 dB

=== Input Noise Ch.1-2 (200 Ohm Source, 60dB Gain, 20kHz BW) ===
ripple (20Hz..20000Hz) L=0.022 dB, R=0.026 dB
dynamic:  L=81.6 dB,     R=81.6 dB
equivalent input noise:  L=-127.6 dBu,  R=-127.6 dBu

=== Write EEPROM ===

update serial number: 809691011
reading old IDs:
  type: 5230
  Xilinx bitfile: 5230
  hardware revision: 1
  production code: 9691
  serial number: 809691011
  test date: 26-Sep-2008 14:09:52
writing new IDs:
  type: 5230
  Xilinx bitfile: 5230
  hardware revision: 1
  production code: 9691
  serial number: 809691011
  test date: 26-Sep-2008 14:13:46
caldata =
   253
    10
    16
     0
   216
   166
    85
    35
     7
     9
    15
     0
   217
   167
    86
    36
    11
     0
```

```
     0
     0
   217
   168
    86
    37
    22
     0
     0
     0
   218
   168
    87
    37
elapsed_time =
       34.281
```

Pin Assignment



Pin out for the 52-5230 Module.

52-5240A - MB/CR/XD Analog In/Out Module

Technical Specifications

A/D Converter

max. input level:	18 dBu (balanced)
input impedance:	approx. 10 kOhm
frequency response:	< 0.1 dB
THD+N:	< -107 dBFS (-30 dBFS, -15 dBu test signal level)
	< -105 dBFS (-9 dBFS, +6 dBu test signal level)
	< -95 dBFS (-1 dBFS, +14 dBu test signal level)
crosstalk:	< -110 dB (1kHz)
dynamic range:	110dB (A-weighted, 0 dBFS = +15 dBu)
common mode rejection:	> 60 dB
converter technology:	24 bit, oversampling sigma-delta

D/A Converter

max. output level (phones, single ended):	18 dBu (balanced)
output impedance:	approx. 25 Ohm
minimum load (outputs short circuit protected):	600 Ohm
frequency response:	< 0.1 dB
THD+N:	< -106 dBFS (-30 dBFS, -15 dBu test signal level), (< -91 dBu)
	< -103 dBFS (-9 dBFS, +6 dBu test signal level), (< -88 dBu)
	< -90 dBFS (-1 dBFS, +14 dBu test signal level), (< -75 dBu)

D/A Converter

crosstalk:	< -110 dB
dynamic range:	109 dB (A-weighted, 0 dBFS = +15 dBu)
DC offset voltage:	< 30 mV
common mode rejection (output impedance):	> 60 dB
common mode rejection (output voltage):	> 40 dB
converter technology:	24 bit, oversampling sigma-delta

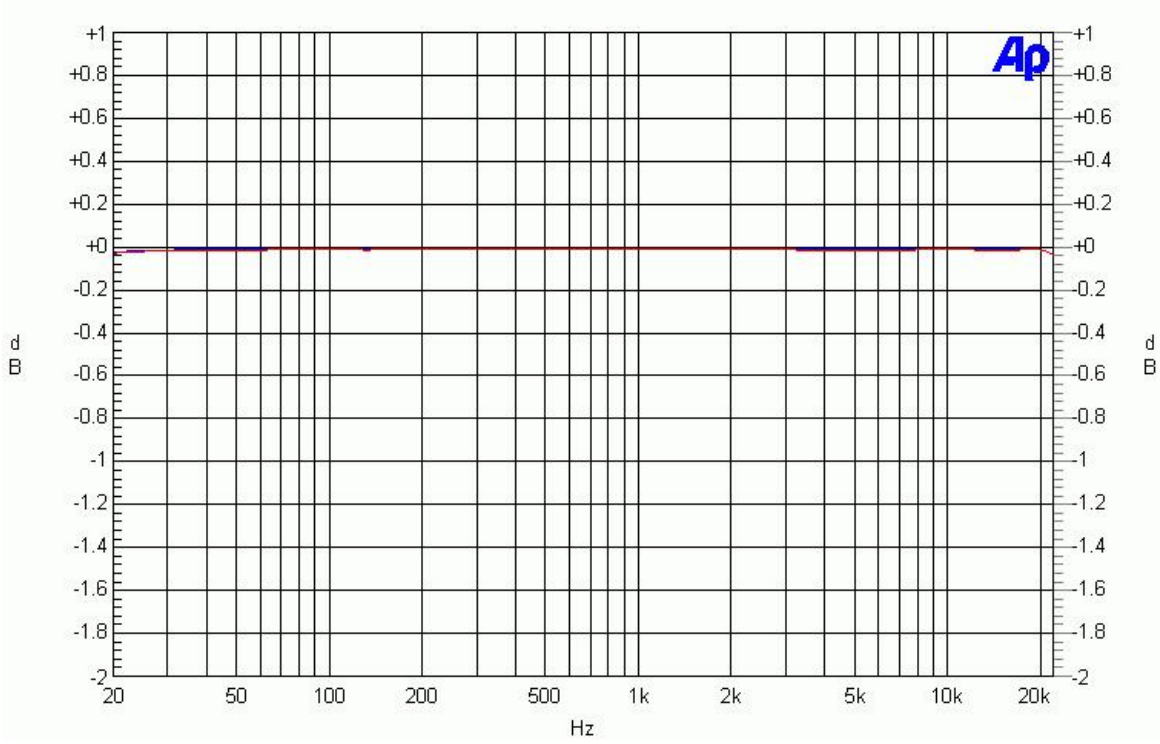
Further Information

power consumption:	3.6 W (typical)
connector style:	XLR 5-pin connectors
printed circuit board (PCB) revision for this specifications:	2

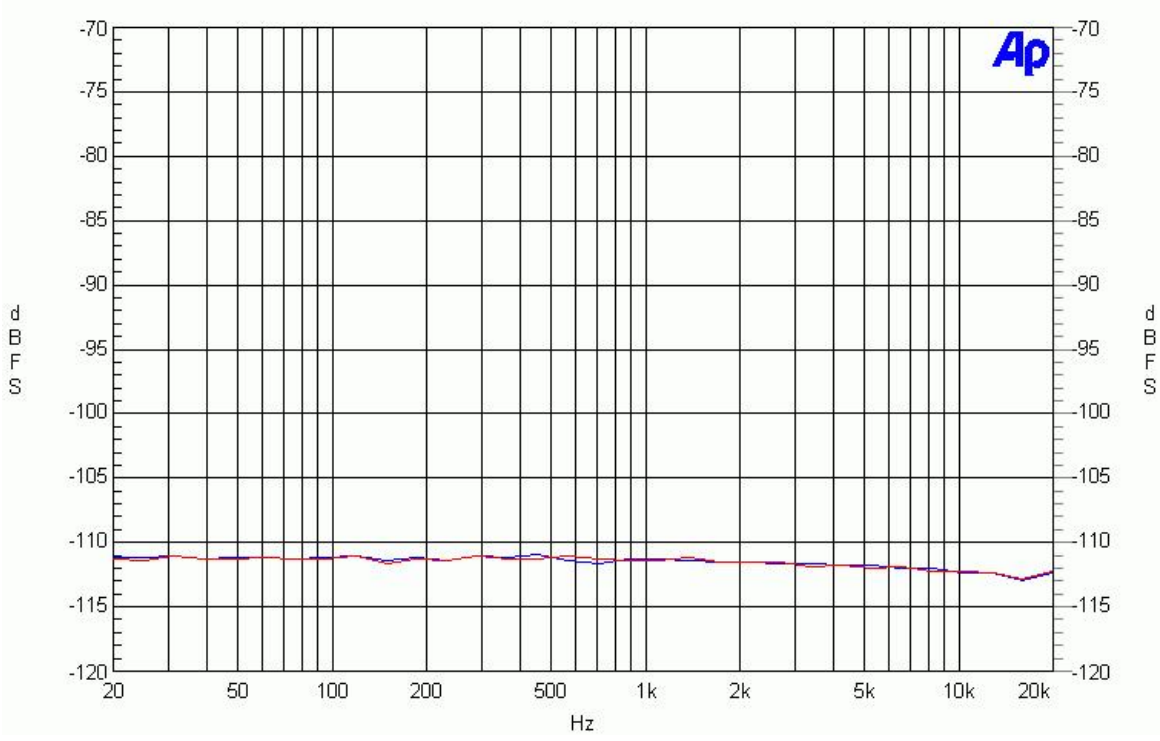
Note

All values are typical values, regarding the factory test limits, you can find in the log file example.

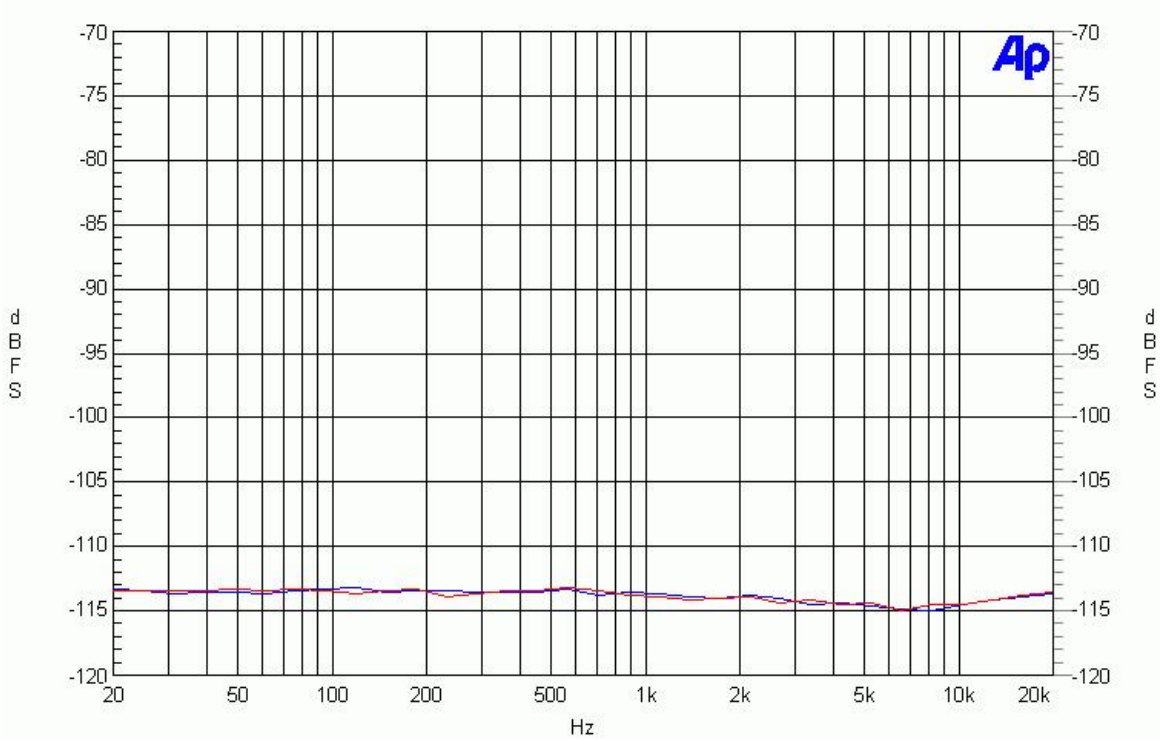
Measurement Plots 52-5240A Inputs



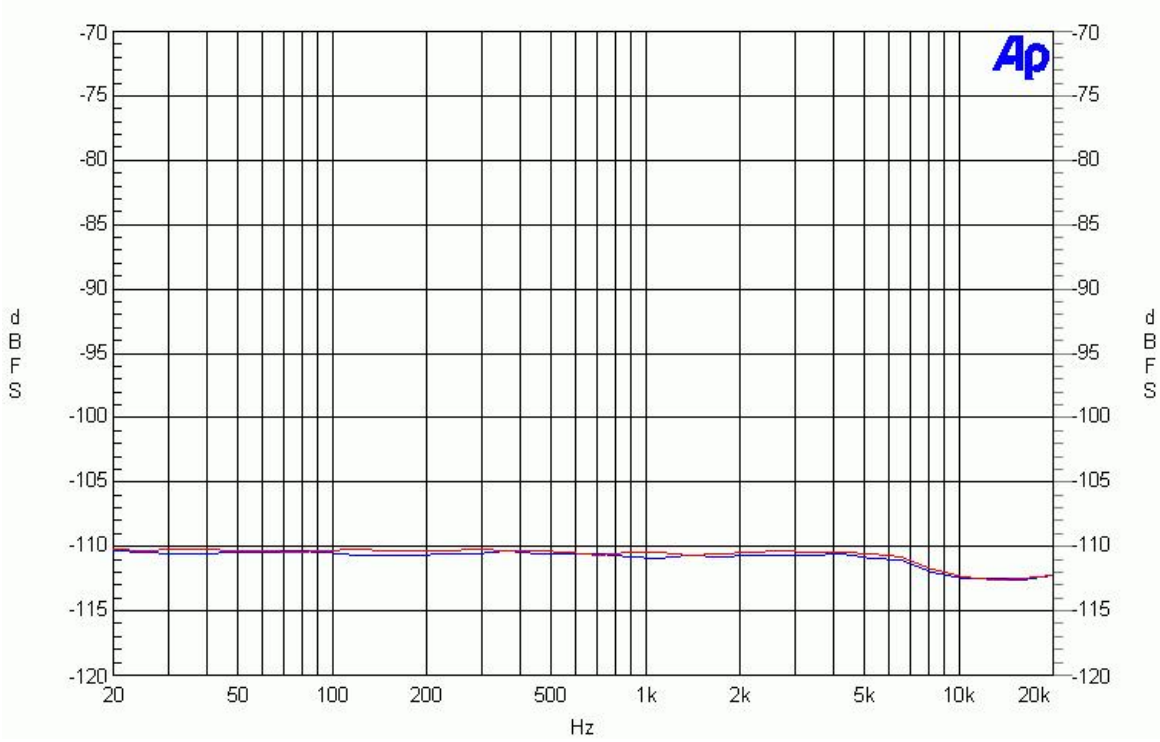
52-5240A ADC Frequency Response



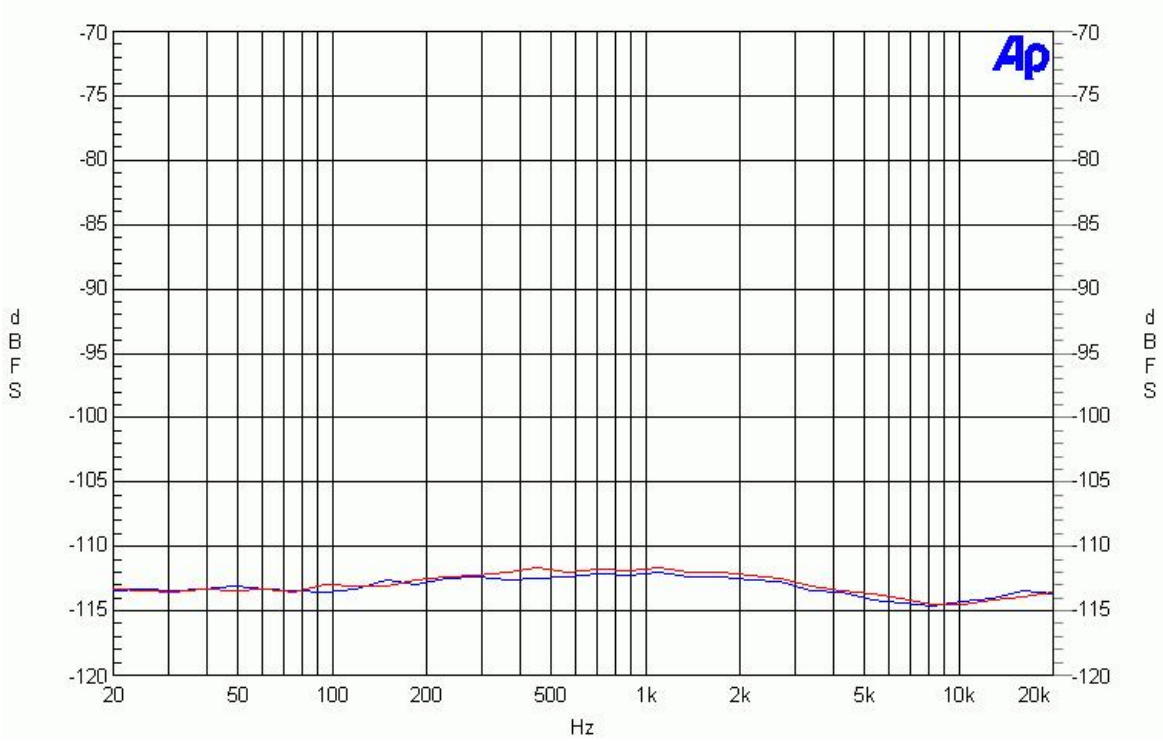
52-5240A ADC THD+N @ -30 dBFS



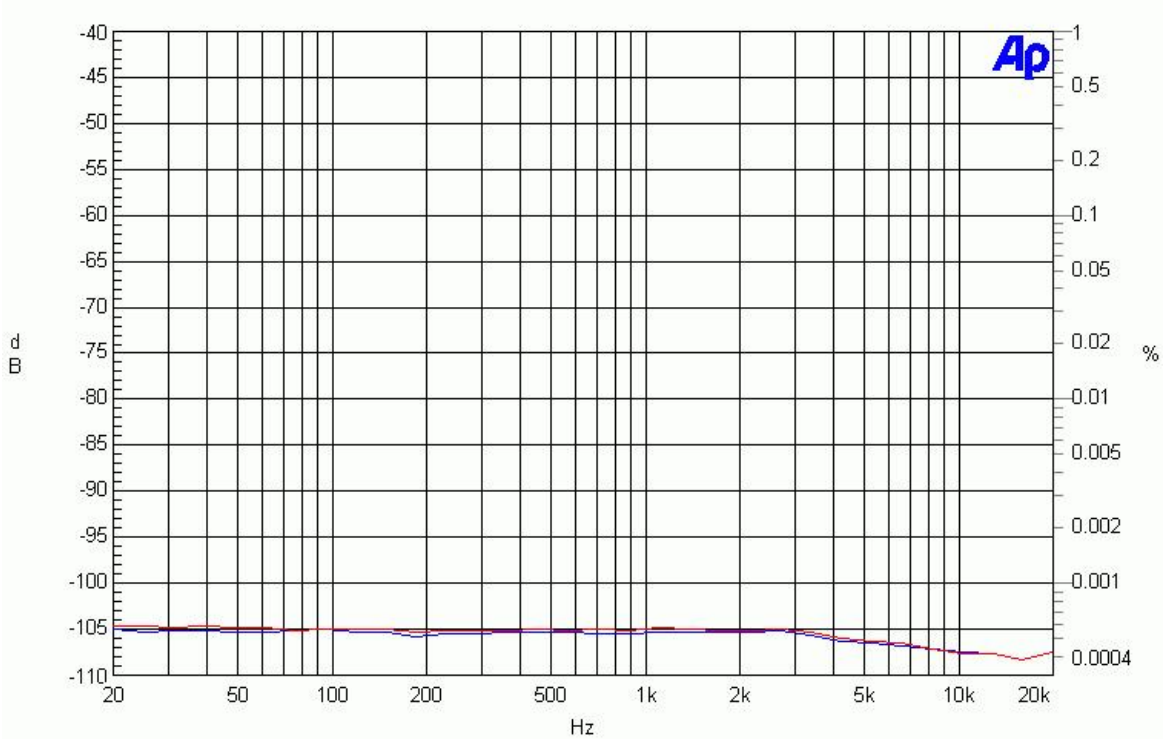
52-5240A ADC THD+N(A) @ -30 dBFS



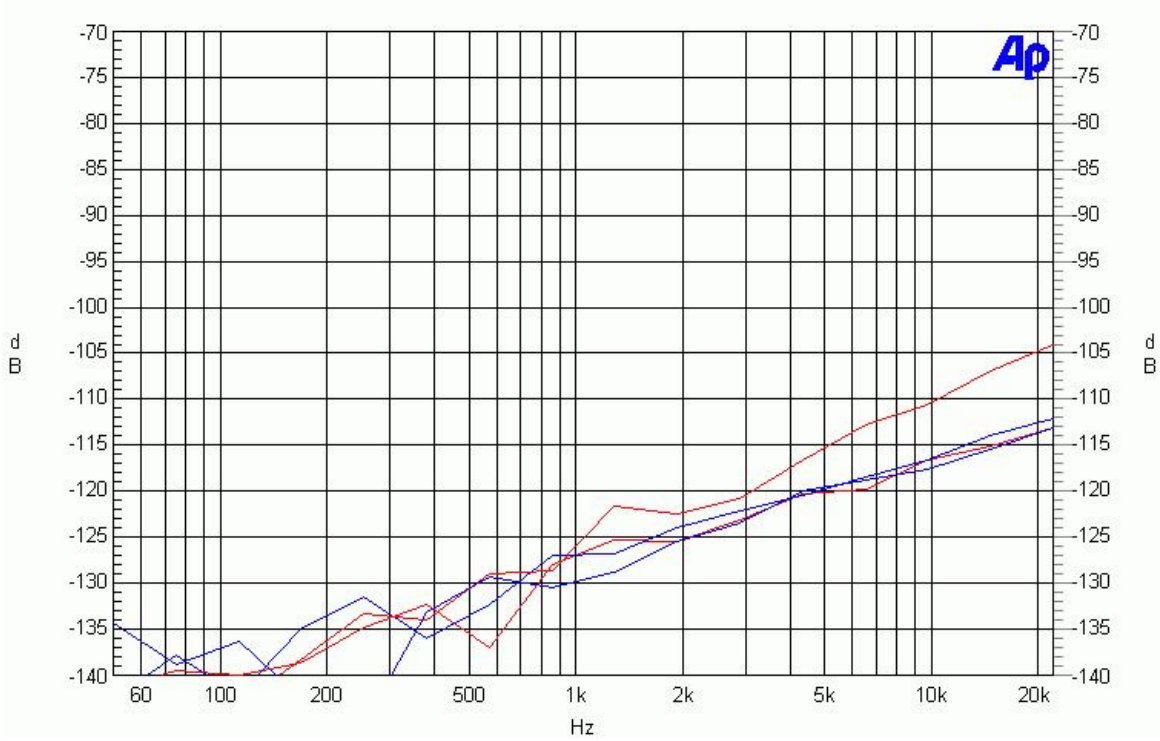
52-5240A ADC THD+N @ +6 dBu



52-5240A ADC THD+N(A) @ + 6 dBu

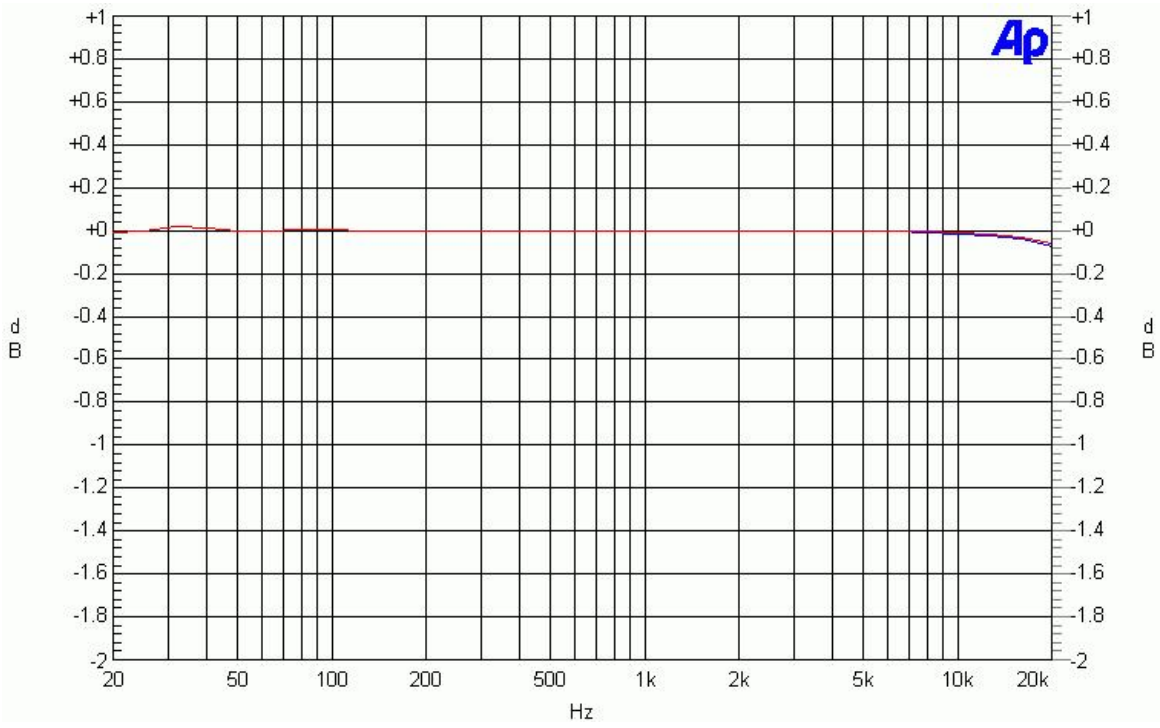


52-5240A ADC THD+N @ +14 dBu

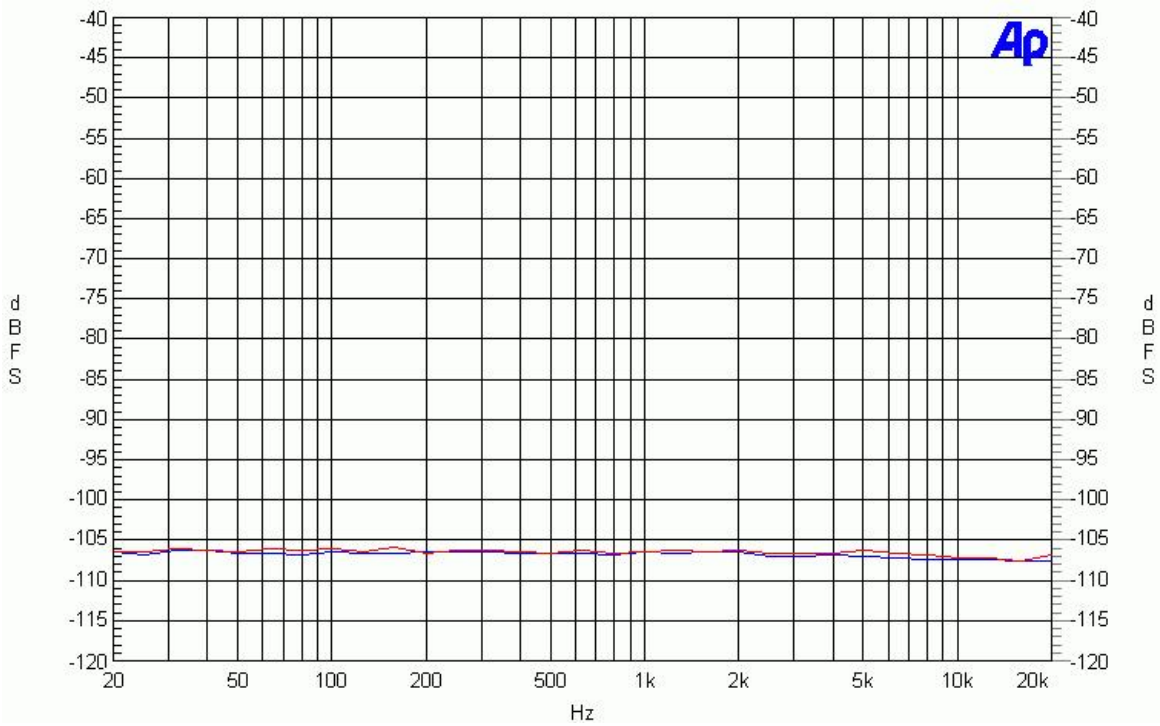


52-5240A ADC Cross-Talk

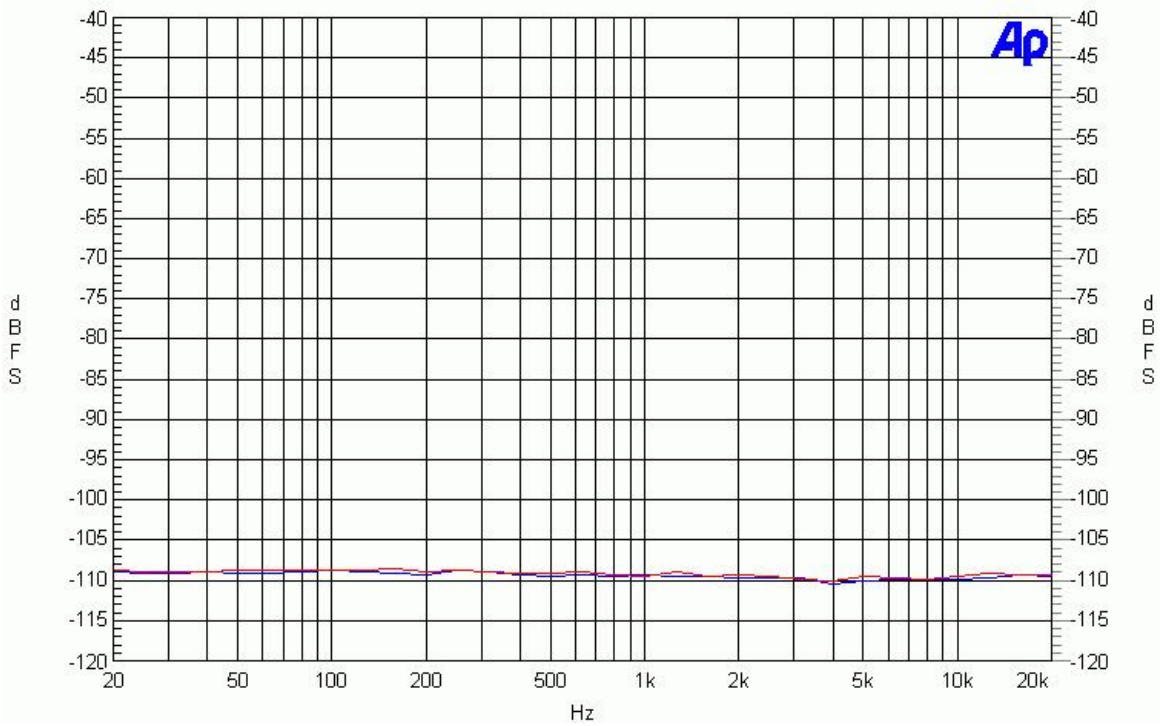
Measurement Plots 52-5240A Outputs



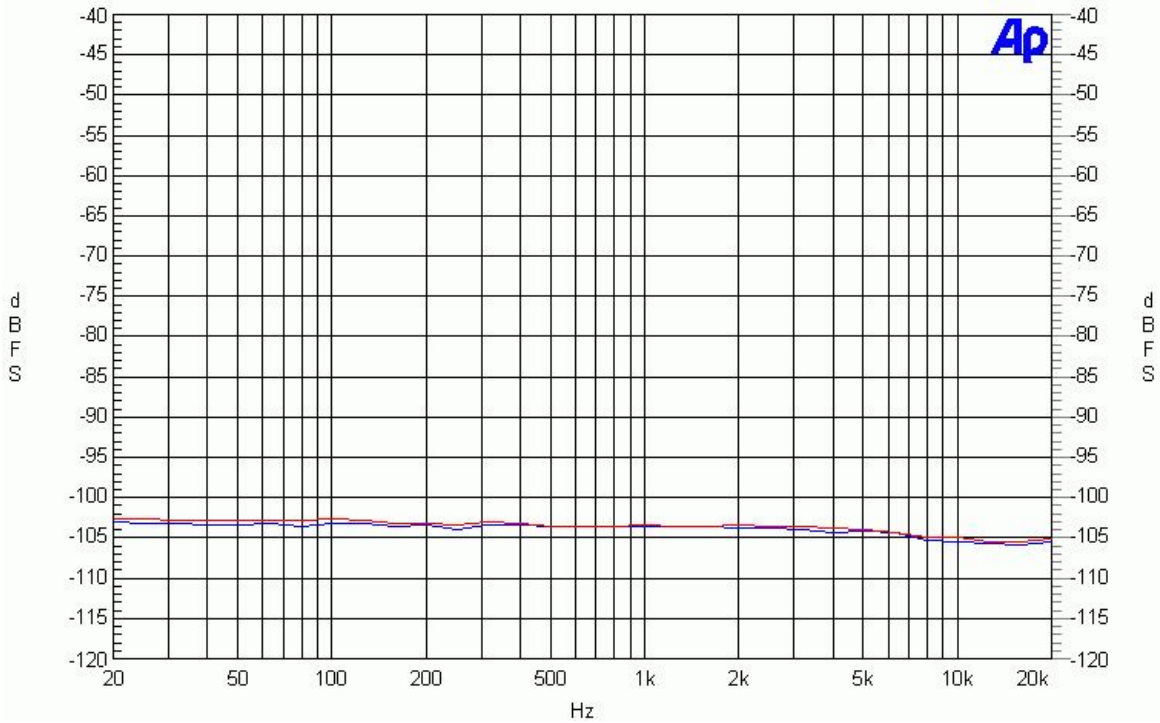
52-5240A DAC Frequency Response



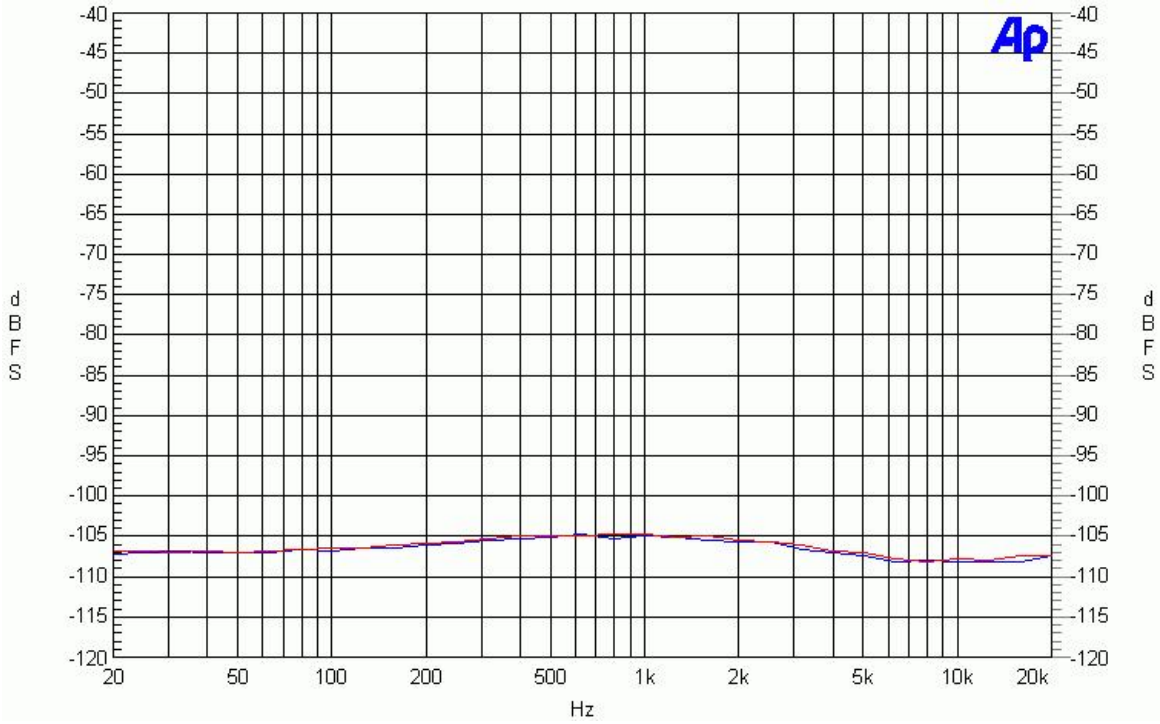
52-5240A DAC THD+N @ -30 dBFS



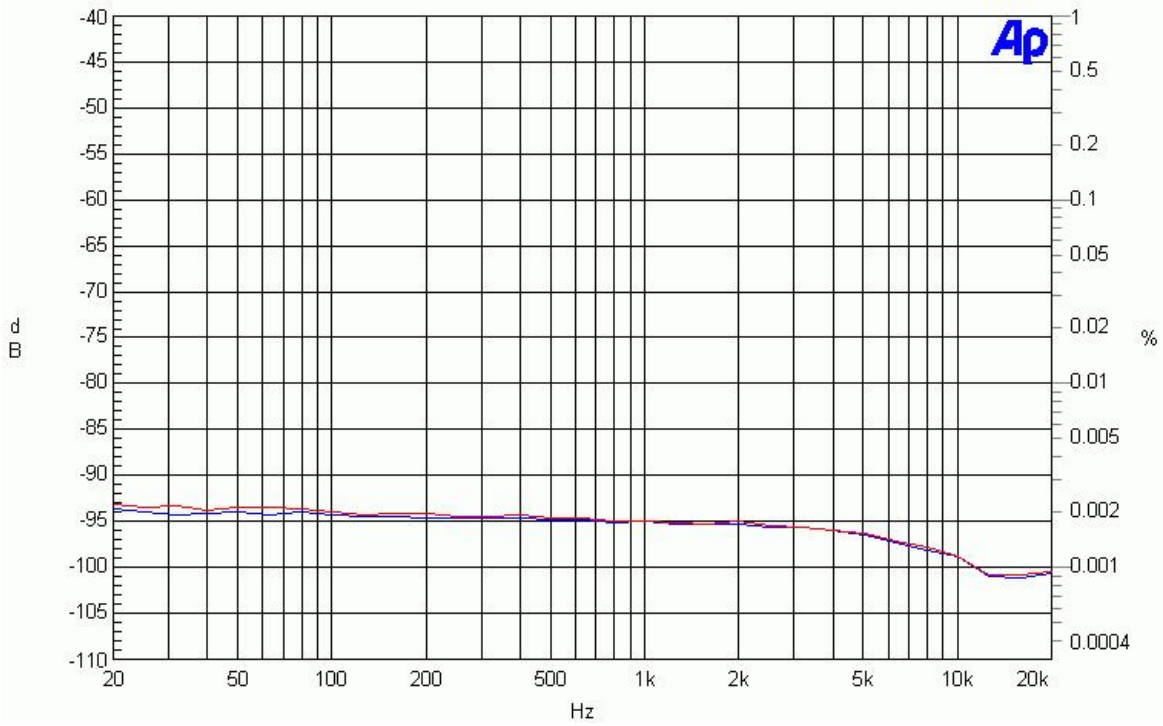
52-5240A DAC THD+N(A) @ -30 dBFS



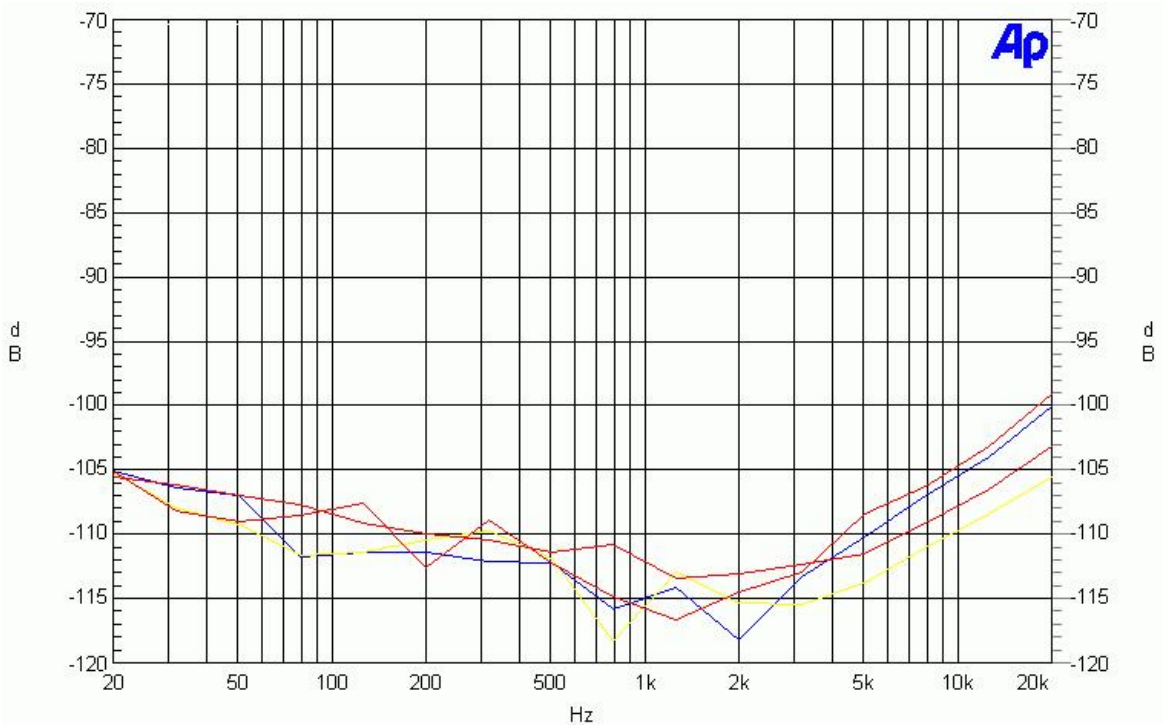
52-5240A DAC THD+N @ +6 dBu



52-5240A DAC THD+N(A) @ +6 dBu



52-5240A DAC THD+N @ +14 dBu



52-5240A DAC Cross-Talk

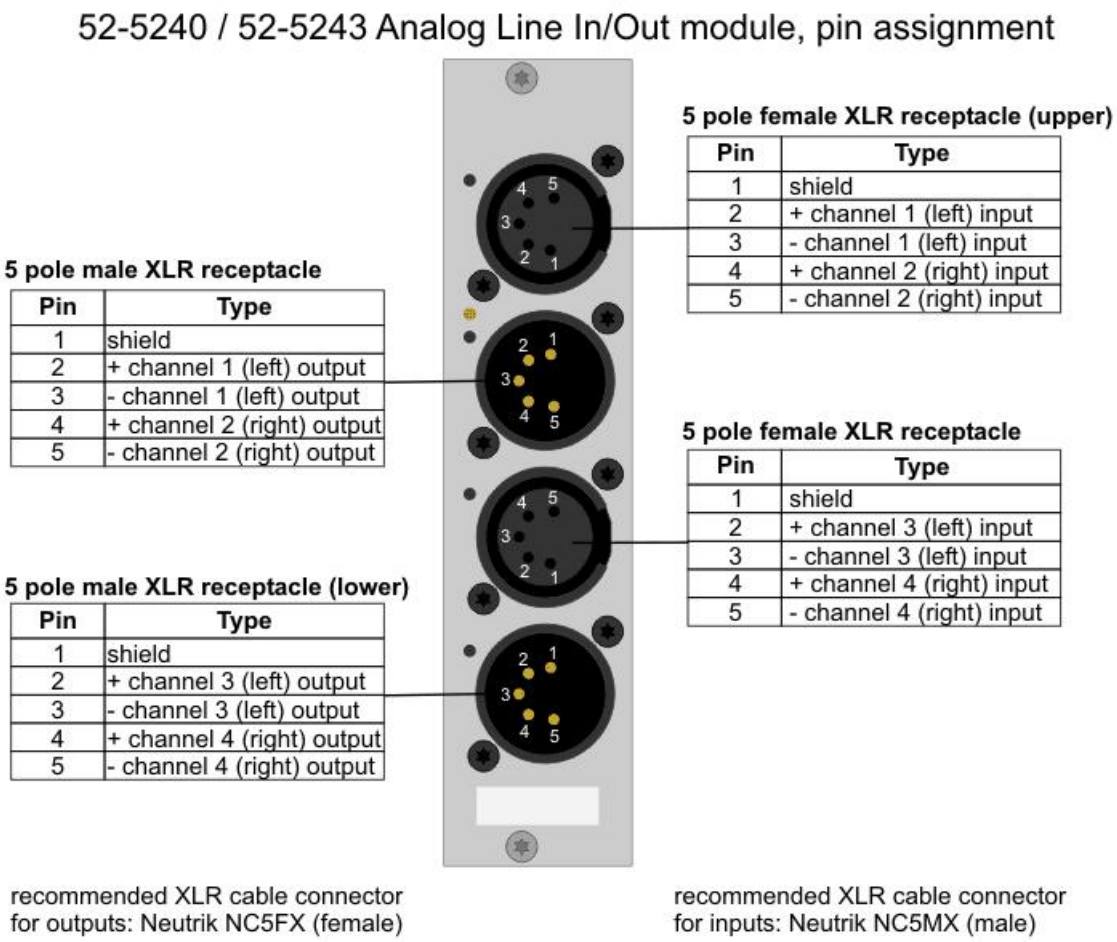
Log File Example

After manufacturing all inputs and outputs of every I/O card are measured. Hence, we can make sure that every module, leaving the production hall, is working correctly. During this process a log file is written. This file is saved by DHD for maintenance purposes.

In the following you can find a log file example of an 52-5240 module:

```
test protocol: z52-52401
serial number: 606446033
production code: 6446
test date: 02-May-2007 12:47:43

ADC frequency response (abs.max. ripple 20Hz..20kHz)
Limit: -0.05 dB .. +0.02 dB
  Ch1: 0.01 dB
  Ch2: 0.01 dB
  Ch3: 0.01 dB
  Ch4: 0.01 dB
ADC dynamic range:
Limit: +109 dB .. +Inf dB
  Ch1: 111.4 dB
  Ch2: 111.3 dB
  Ch3: 111.4 dB
  Ch4: 111.4 dB
ADC multitone distortions and noise:
Limit: -Inf dB .. -98 dB
  Ch1: -105.2 dB
  Ch2: -104.6 dB
  Ch3: -100.2 dB
  Ch4: -101.2 dB
ADC common mode rejection (20Hz..15kHz, worst case):
Limit: 58 dB .. Inf dB
  Ch1: 77 dB
  Ch2: 74 dB
  Ch3: 72 dB
  Ch4: 76 dB
DAC frequency response (abs.max. ripple 20Hz..20kHz)
Limit: -0.05 dB .. +0.02 dB
  Ch1: 0.02 dB
  Ch2: 0.02 dB
  Ch3: 0.01 dB
  Ch4: 0.01 dB
DAC dynamic range:
Limit: +108 dB .. +Inf dB
  Ch1: 109.5 dB
  Ch2: 109.8 dB
  Ch3: 109.6 dB
  Ch4: 110.0 dB
DAC multitone distortions and noise (300 Ohm load):
Limit: -Inf dB .. -94 dB
  Ch1: -97.2 dB
  Ch2: -97.1 dB
  Ch3: -97.1 dB
  Ch4: -96.6 dB
DAC output impedance:
Limit: 23 Ohm .. 28 Ohm
  Ch1: 25.1 Ohm
  Ch2: 25.0 Ohm
  Ch3: 24.9 Ohm
  Ch4: 24.9 Ohm
DAC common mode rejection (20Hz..15kHz, worst case):
Limit: 40 dB .. Inf dB
  Ch1: 53 dB
  Ch2: 67 dB
  Ch3: 55 dB
  Ch4: 54 dB
power supplies:
  VCC1V2: 1.22 V
  VCC2V5: 2.55 V
  VCC3  : 3.27 V
  VCC5  : 4.99 V
  VANALOG: 7.9 V
```

Pin Assignment



Pin out for the 52-5240 Module.

52-5243A - MB/CR/XD Analog In/Out Module

Technical Specifications

A/D Converter

max. input level:	24 dBu (balanced)
input impedance:	approx. 10 kOhm
frequency response:	< 0.1 dB
THD+N:	< -110 dBFS (-30 dBFS, -6 dBu test signal level)
	< -110 dBFS (-20 dBFS, +4 dBu test signal level)
	< -90 dBFS (-1 dBFS, +23 dBu test signal level)
crosstalk:	< -110 dB
dynamic range:	113 dB (A-weighted, 0 dBFS = +24 dBu)
common mode rejection:	> 60 dB
converter technology:	24 bit, oversampling sigma-delta

D/A Converter

max. output level (phones, single ended):	24 dBu (balanced)
output impedance:	approx. 25 Ohm
minimum load (outputs short circuit protected):	600 Ohm
frequency response:	< 0.1 dB
THD+N:	< -109 dBFS (-30 dBFS, -6 dBu test signal level), (< -85 dBu)
	< -100 dBFS (-20 dBFS, +4 dBu test signal level), (< -76 dBu)
	< -85 dBFS (-1 dBFS, +23 dBu test signal level), (< -61 dBu)

D/A Converter

crosstalk:	< -105 dB
dynamic range:	112 dB (A-weighted, 0dBFS = +24 dBu)
DC offset voltage:	< 30 mV
common mode rejection (output impedance):	> 60 dB
common mode rejection (output voltage):	> 40 dB
converter technology:	24 bit, oversampling sigma-delta

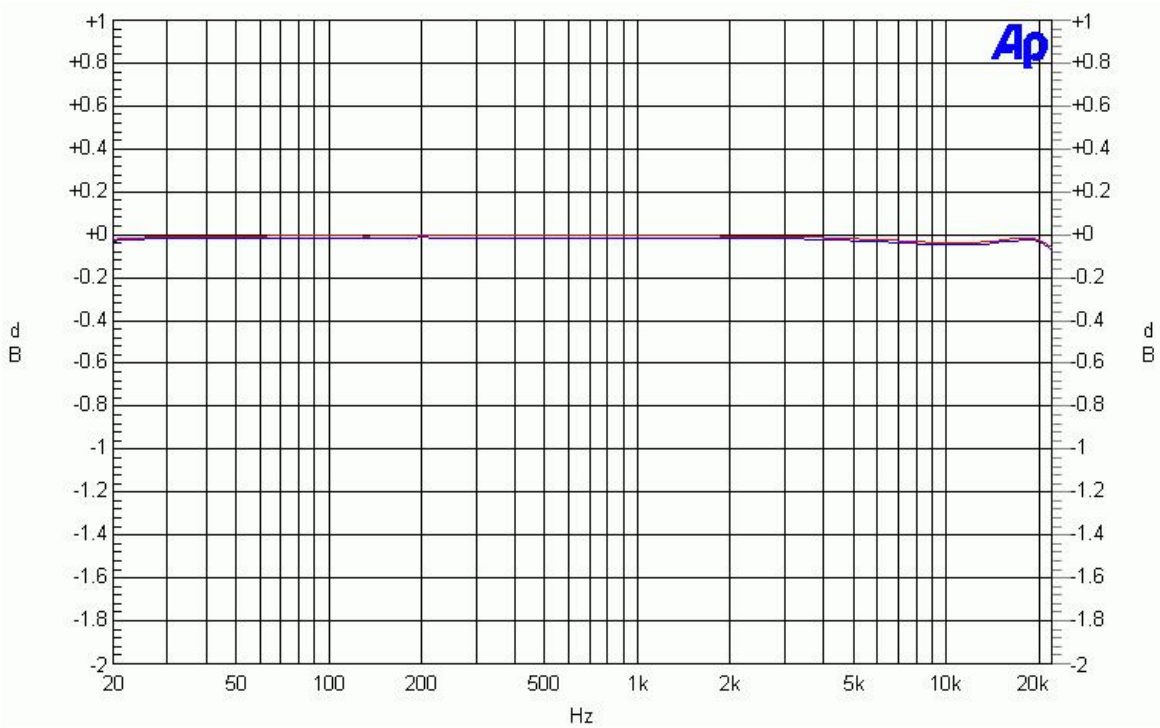
Further Information

power consumption:	5.4 W (typical)
connector style:	XLR 5-pin connectors
printed circuit board (PCB) revision for this specifications:	2

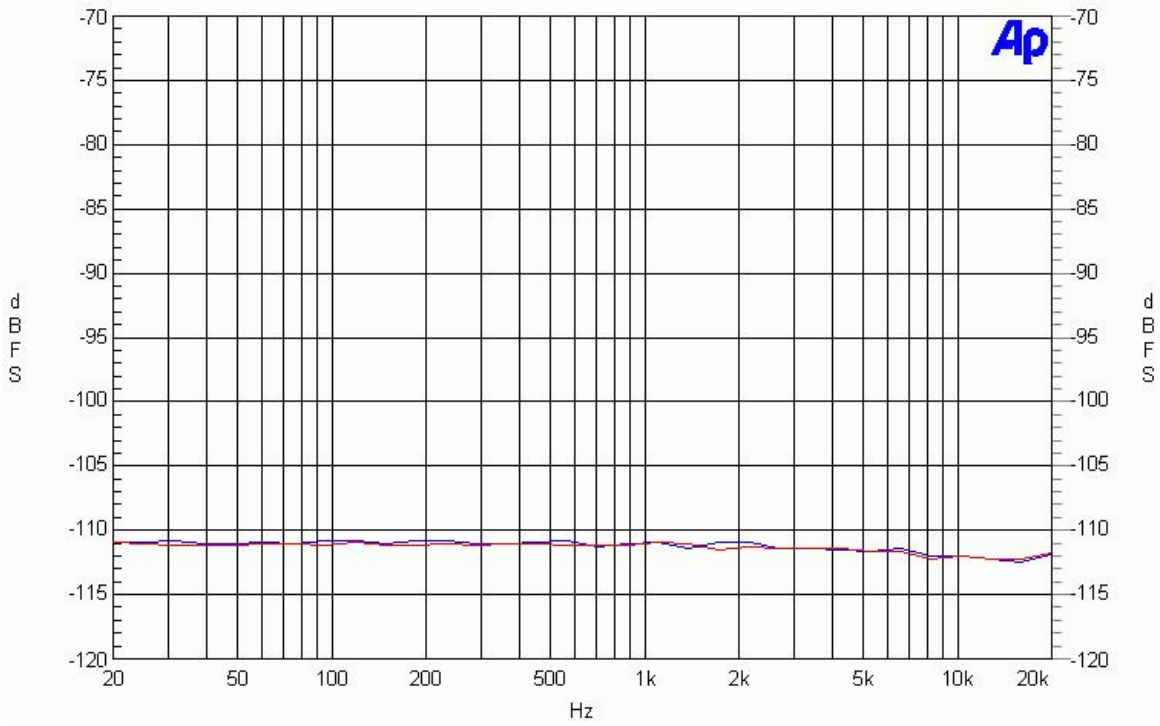
Note

All values are typical values, regarding the factory test limits, you can find in the log file example.

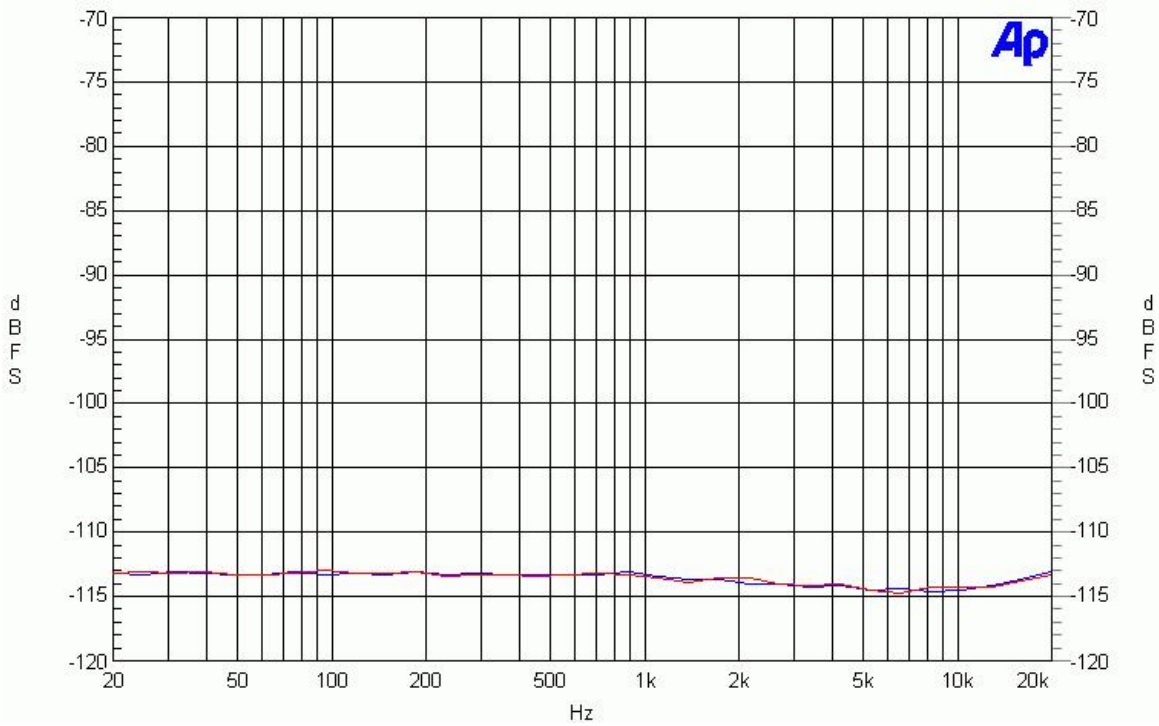
Measurement Plots 52-5243A Inputs



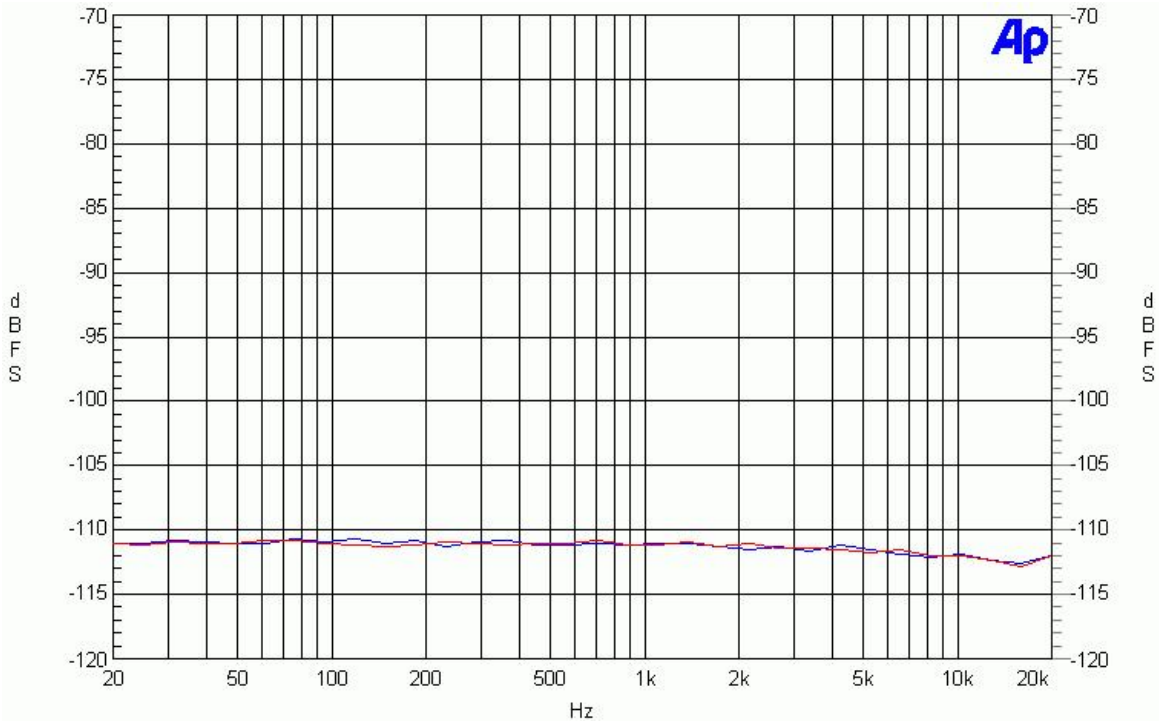
52-5243A ADC Frequency Response



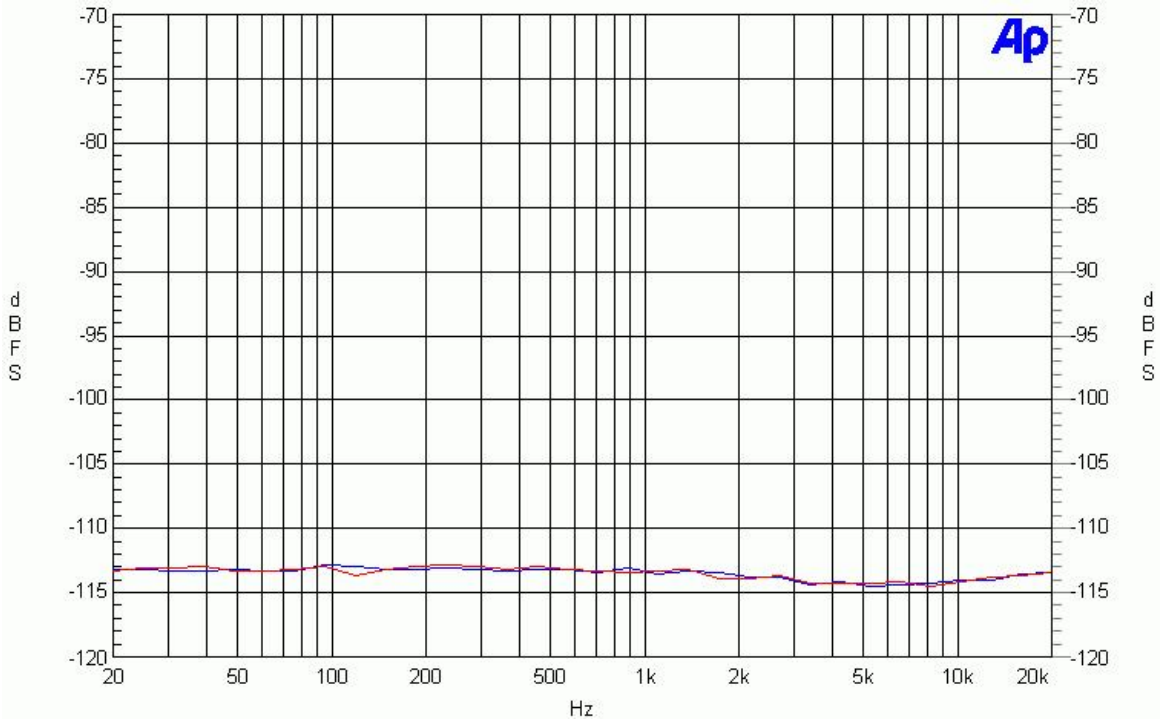
52-5243A ADC THD+N @ -30 dBFS



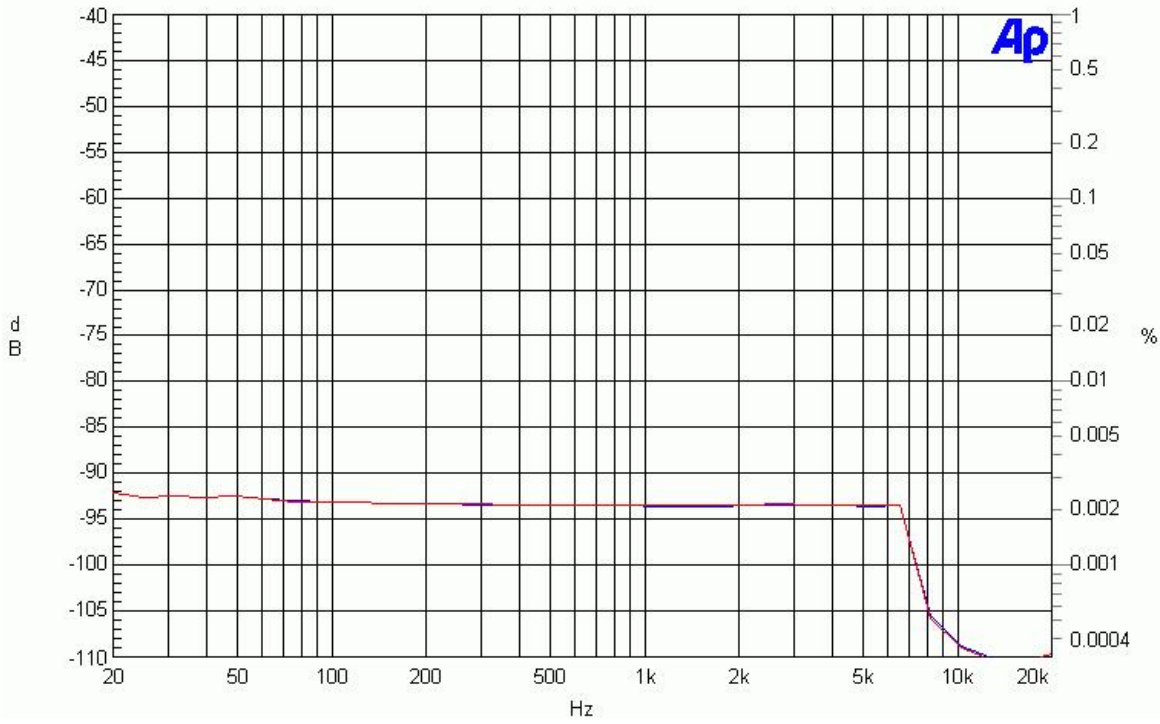
52-5243A ADC THD+N(A) @ -30 dBFS



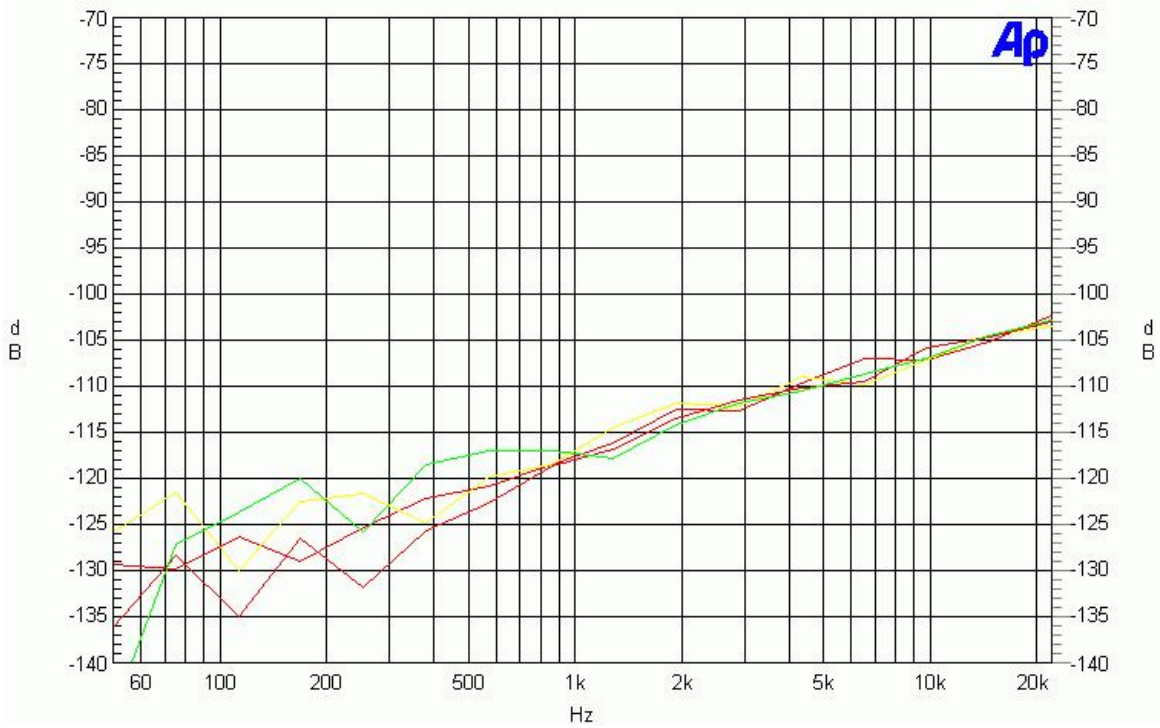
52-5243A ADC THD+N @ +4 dBu



52-5243A ADC THD+N(A) @ +4 dBu

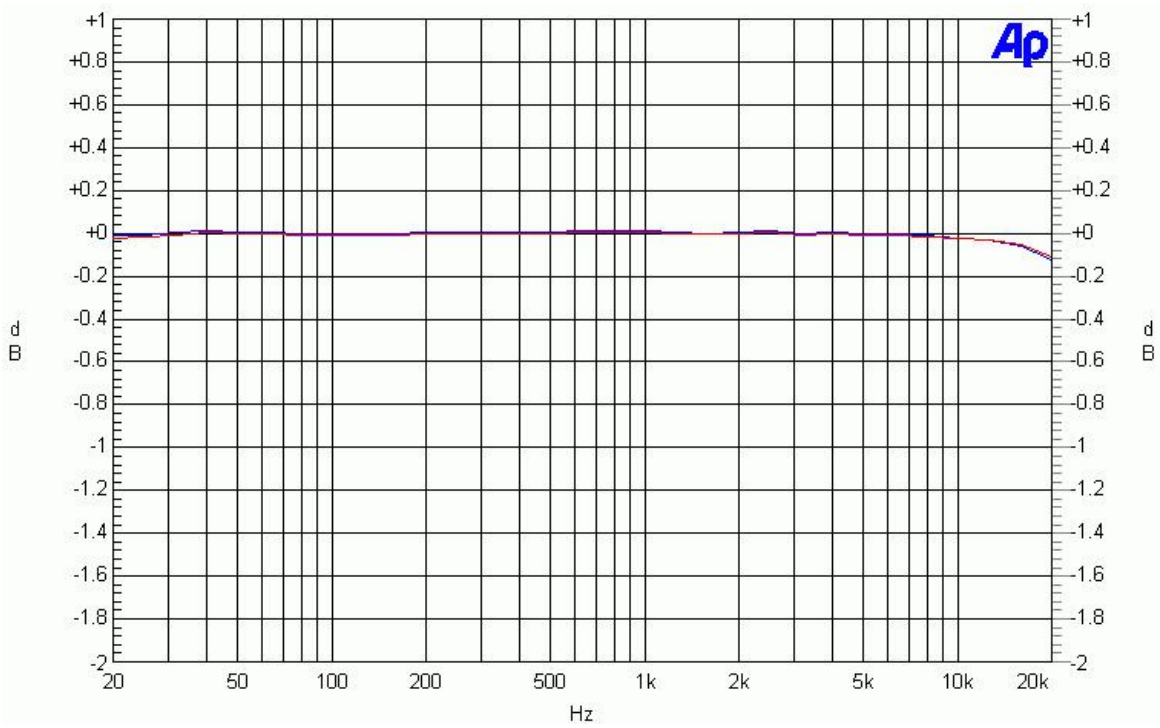


52-5243A ADC THD+N @ +23 dBu

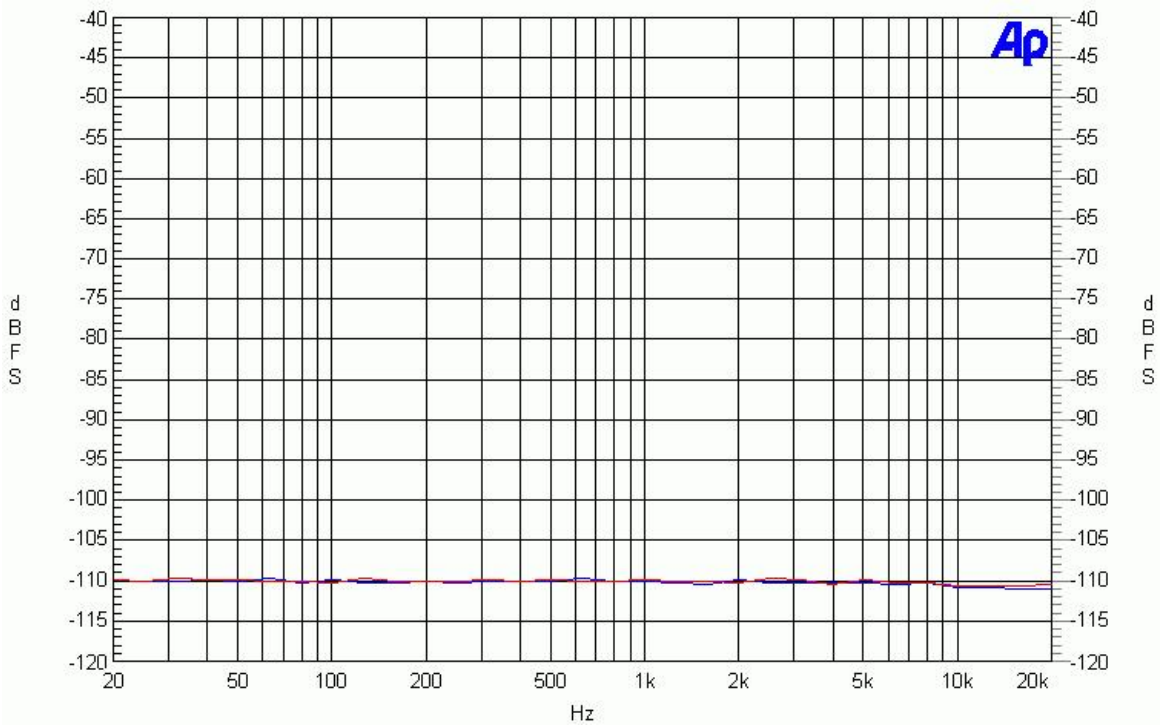


52-5243A ADC Cross-Talk

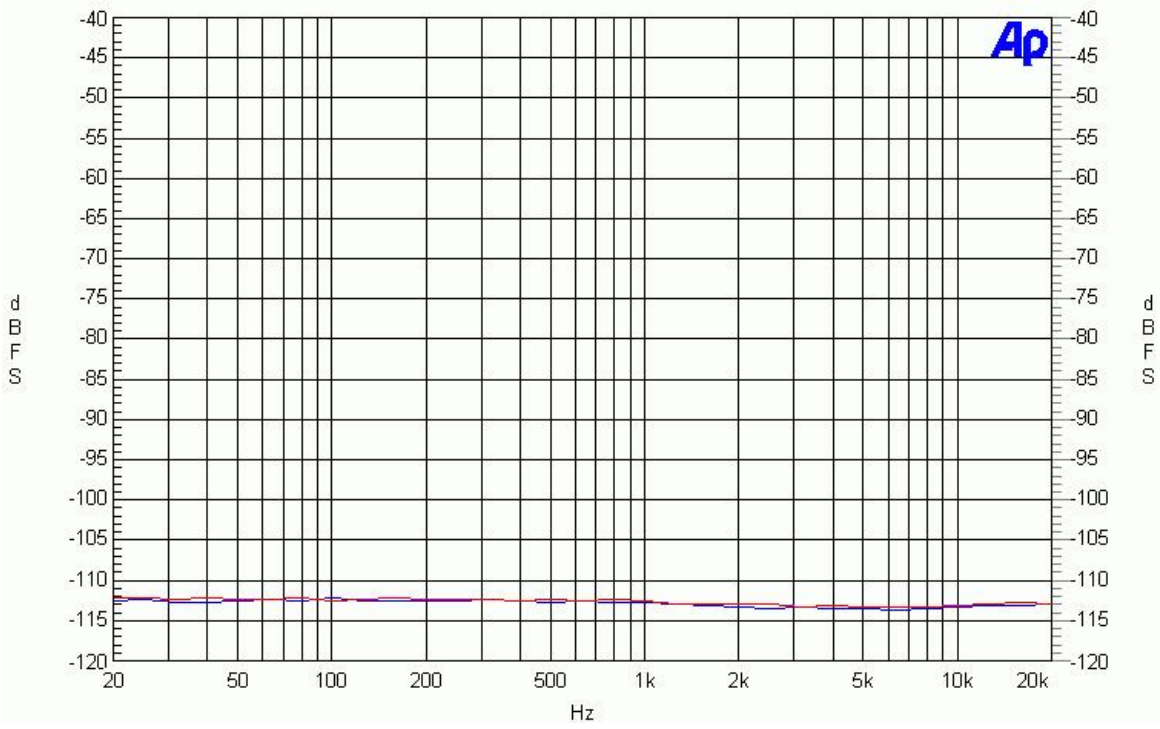
Measurement Plots 52-5243A Outputs



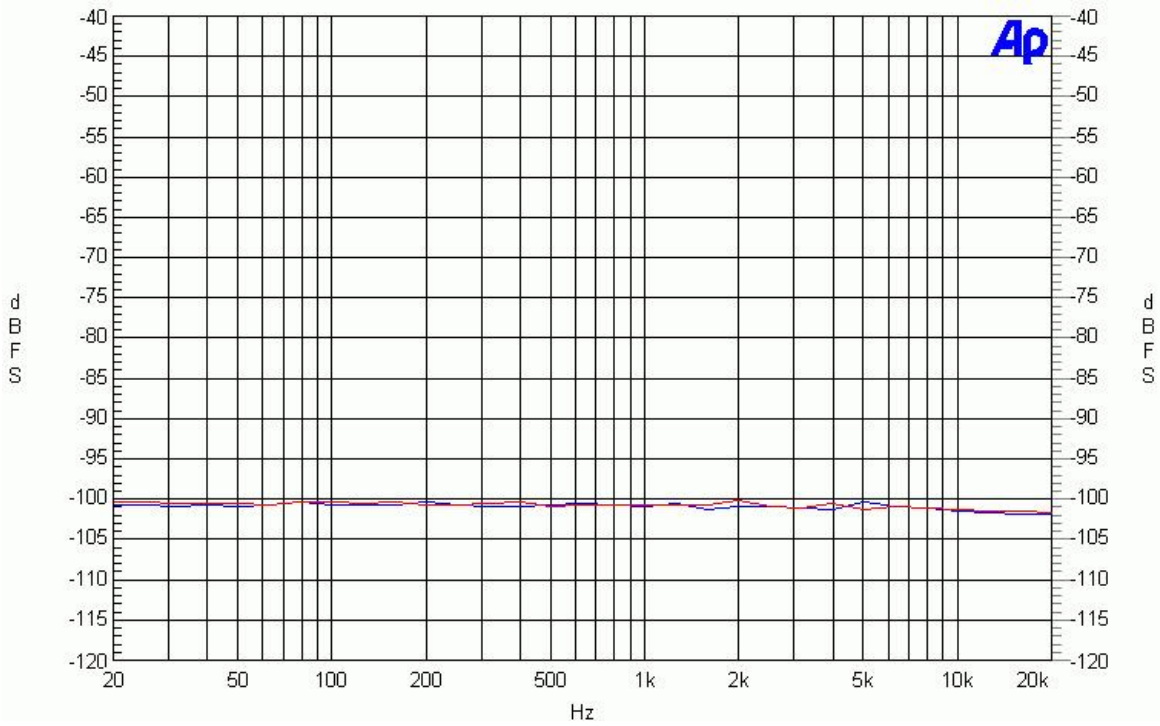
52-5243A DAC Frequency Response



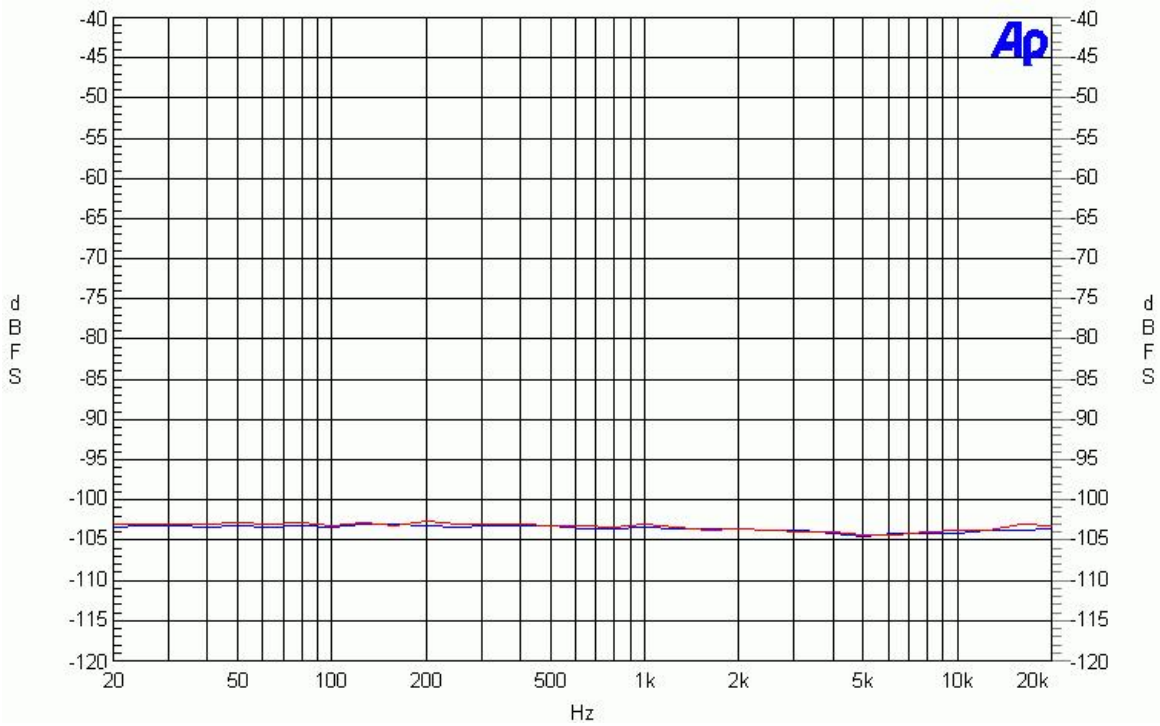
52-5243A DAC THD+N @ -30 dBFS



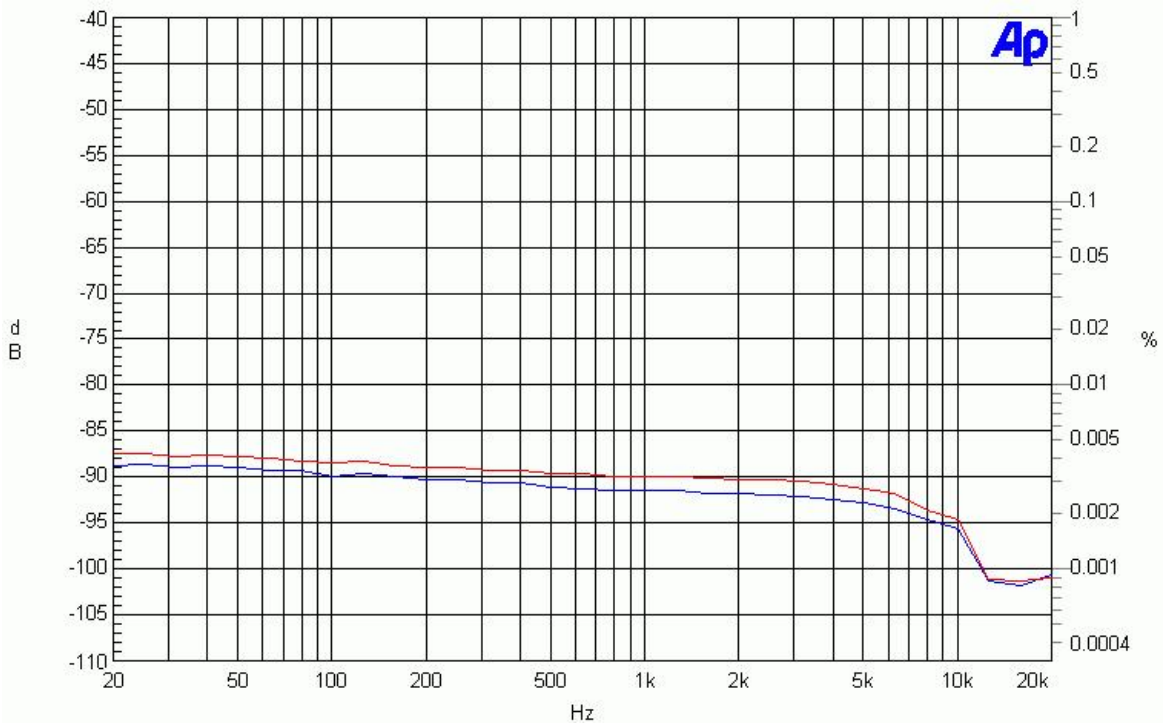
52-5243A DAC THD+N(A) @ -30 dBFS



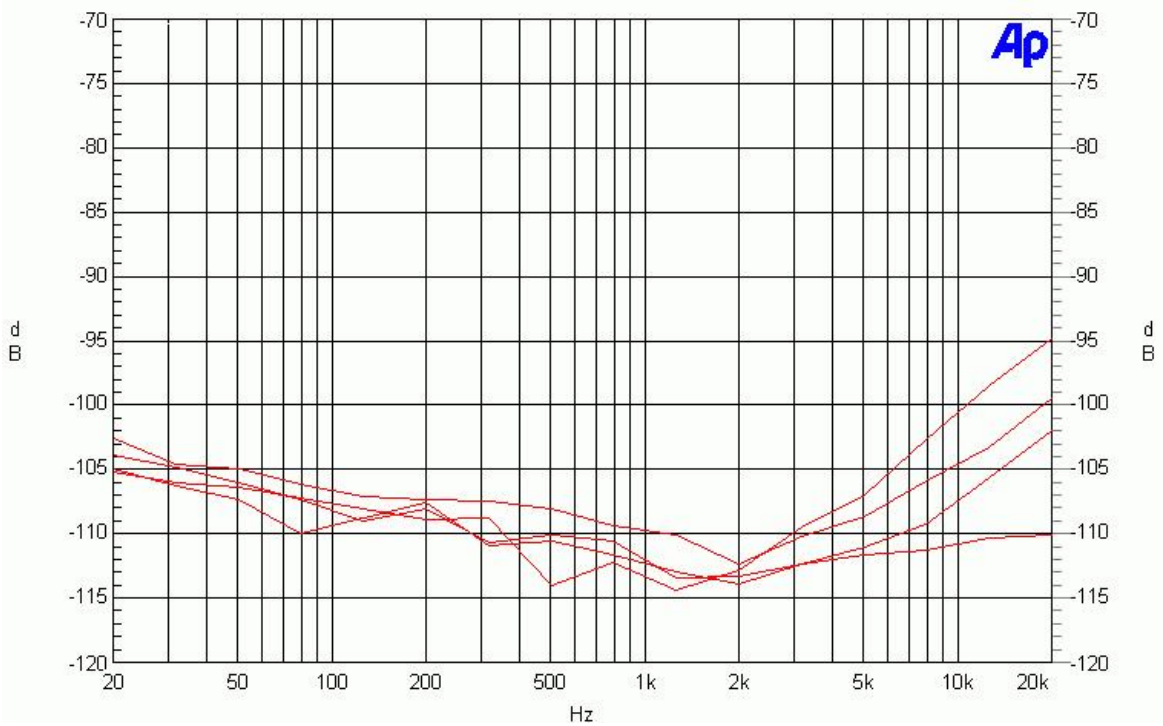
52-5243A DAC THD+N @ +4 dBu



52-5243A DAC THD+N(A) @ +4 dBu



52-5243A DAC THD+N @ -1 dBFS



52-5243A DAC Cross-Talk

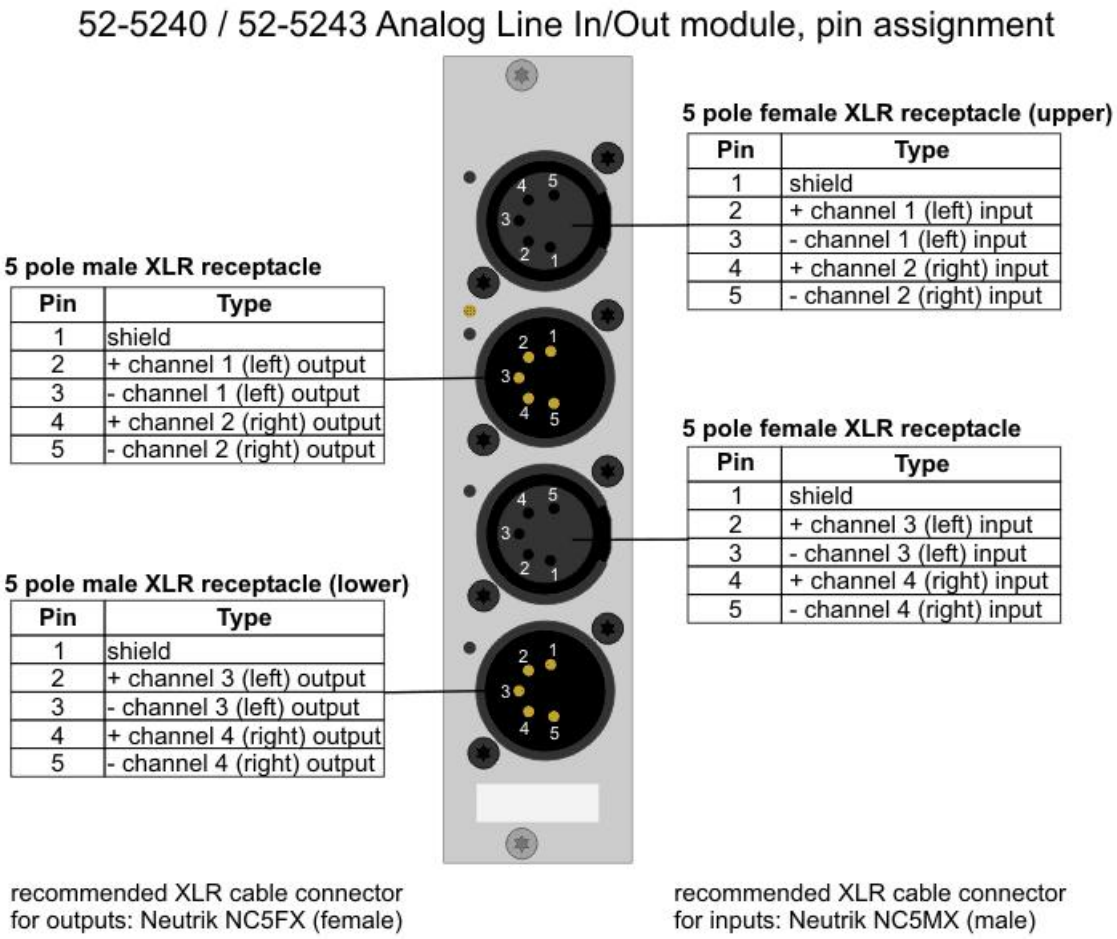
Log File Example

After manufacturing all inputs and outputs of every I/O card are measured. Hence, we can make sure that every module, leaving the production hall, is working correctly. During this process a log file is written. This file is saved by DHD for maintenance purposes.

In the following you can find a log file example of an 52-5243 module:

```
test protocol: z52-52431
serial number: 707456040
production code: 7456
test date: 02-May-2007 12:35:44

ADC frequency response (abs.max. ripple 20Hz..20kHz)
Limit: -0.05 dB .. +0.02 dB
  Ch1: 0.02 dB
  Ch2: 0.01 dB
  Ch3: 0.02 dB
  Ch4: 0.01 dB
ADC dynamic range:
Limit: +109 dB .. +Inf dB
  Ch1: 110.7 dB
  Ch2: 110.8 dB
  Ch3: 110.7 dB
  Ch4: 110.8 dB
ADC multitone distortions and noise:
Limit: -Inf dB ..-98 dB
  Ch1: -103.5 dB
  Ch2: -101.4 dB
  Ch3: -101.6 dB
  Ch4: -101.9 dB
ADC common mode rejection (20Hz..15kHz, worst case):
Limit: 58 dB .. Inf dB
  Ch1: 73 dB
  Ch2: 74 dB
  Ch3: 78 dB
  Ch4: 74 dB
DAC frequency response (abs.max. ripple 20Hz..20kHz)
Limit: -0.05 dB .. +0.02 dB
  Ch1: 0.02 dB
  Ch2: 0.02 dB
  Ch3: 0.03 dB
  Ch4: 0.02 dB
DAC dynamic range:
Limit: +108 dB .. +Inf dB
  Ch1: 109.6 dB
  Ch2: 109.6 dB
  Ch3: 109.5 dB
  Ch4: 109.8 dB
DAC multitone distortions and noise (300 Ohm load):
Limit: -Inf dB ..-94 dB
  Ch1: -97.8 dB
  Ch2: -98.0 dB
  Ch3: -96.9 dB
  Ch4: -97.6 dB
DAC output impedance:
Limit: 23 Ohm .. 28 Ohm
  Ch1: 25.1 Ohm
  Ch2: 25.1 Ohm
  Ch3: 24.9 Ohm
  Ch4: 25.1 Ohm
DAC common mode rejection (20Hz..15kHz, worst case):
Limit: 40 dB .. Inf dB
  Ch1: 67 dB
  Ch2: 74 dB
  Ch3: 54 dB
  Ch4: 56 dB
power supplies:
  VCC1V2: 1.22 V
  VCC2V5: 2.52 V
  VCC3  : 3.27 V
  VCC5  : 5.02 V
  VANALOG: 7.8 V
```

Pin Assignment



Pin out for the 52-5243 Module.

52-5250A - MB/CR/XD 4 Mic/Line Module, iso.

Technical Specifications

A/D Converter

max. input level:	26 dBu (balanced)
input impedance:	approx. 5 kOhm
frequency response:	< 0.1 dB
equivalent input noise	< -129 dBu (A-weighted, 200 source impedance, > +30 dB analog gain)
THD+N:	< -112 dBFS (-30 dBFS, +10 dB analog gain) < -100 dBFS (-1 dBFS, +10 dB analog gain)
crosstalk:	< -123 dB (1kHz)
phantom power 48V:	switchable per input channel, unloaded input: 48V +/- 10%
dynamic range:	115 dB (A-weighted, +10 dB analog gain)
common mode rejection:	> 60 dB
converter technology:	24 bit, oversampling sigma-delta

Further Information

power consumption:	3.6 W (typical)
connector style:	XLR 3-pin connectors
printed circuit board (PCB) revision for this specifications:	1

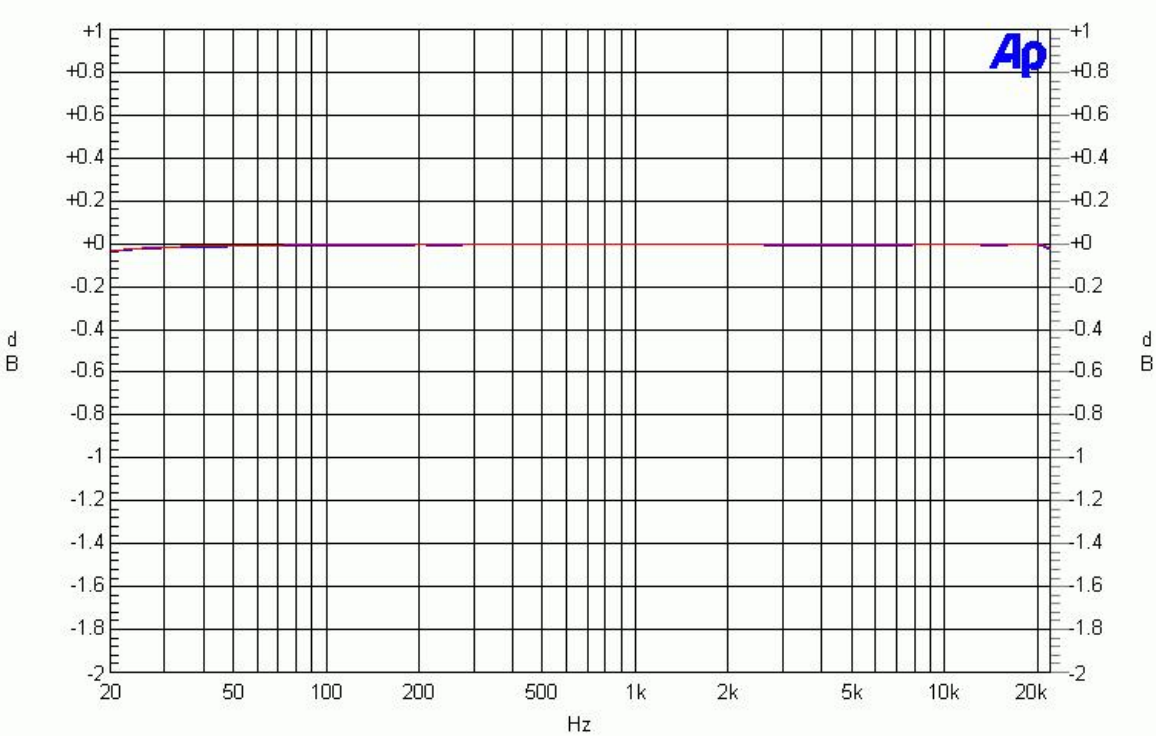
Note

All values are typical values, regarding the factory test limits, you can find in the log file example.

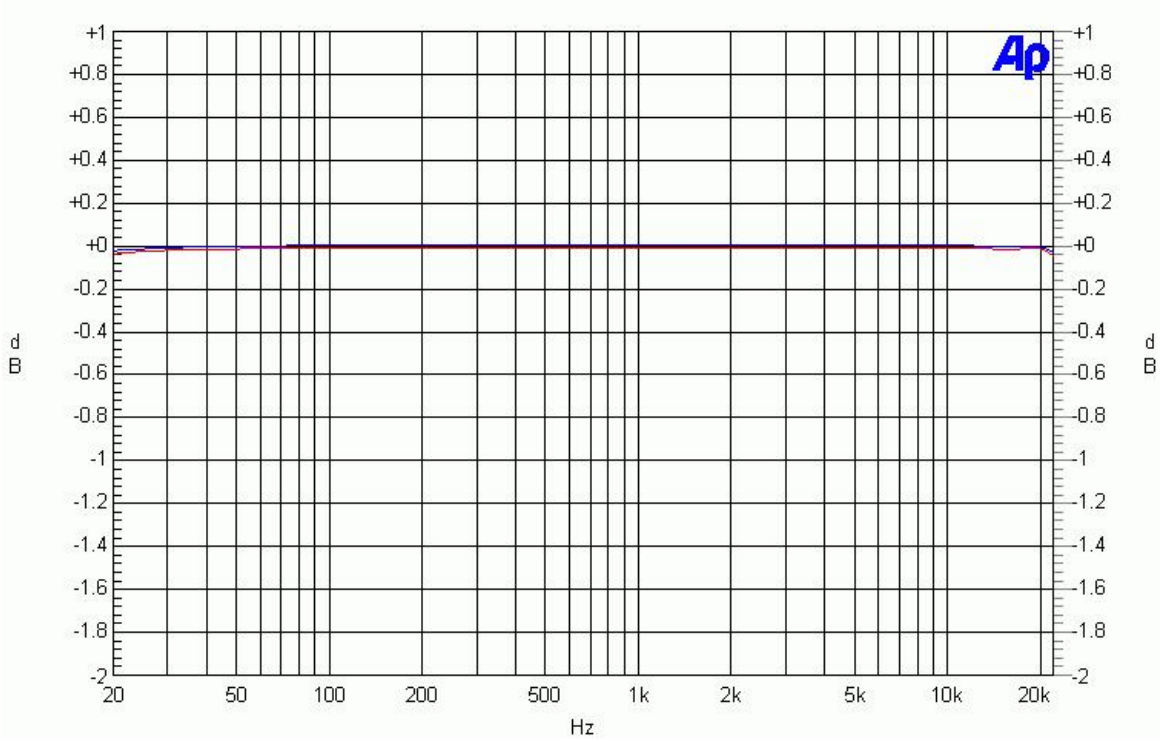
Warning

The wiring of microphone inputs of DHD microphone input modules is not designed to support operation with parallel external phantom power. Using it might result in damages of pre-amplifier or phantom power generator.

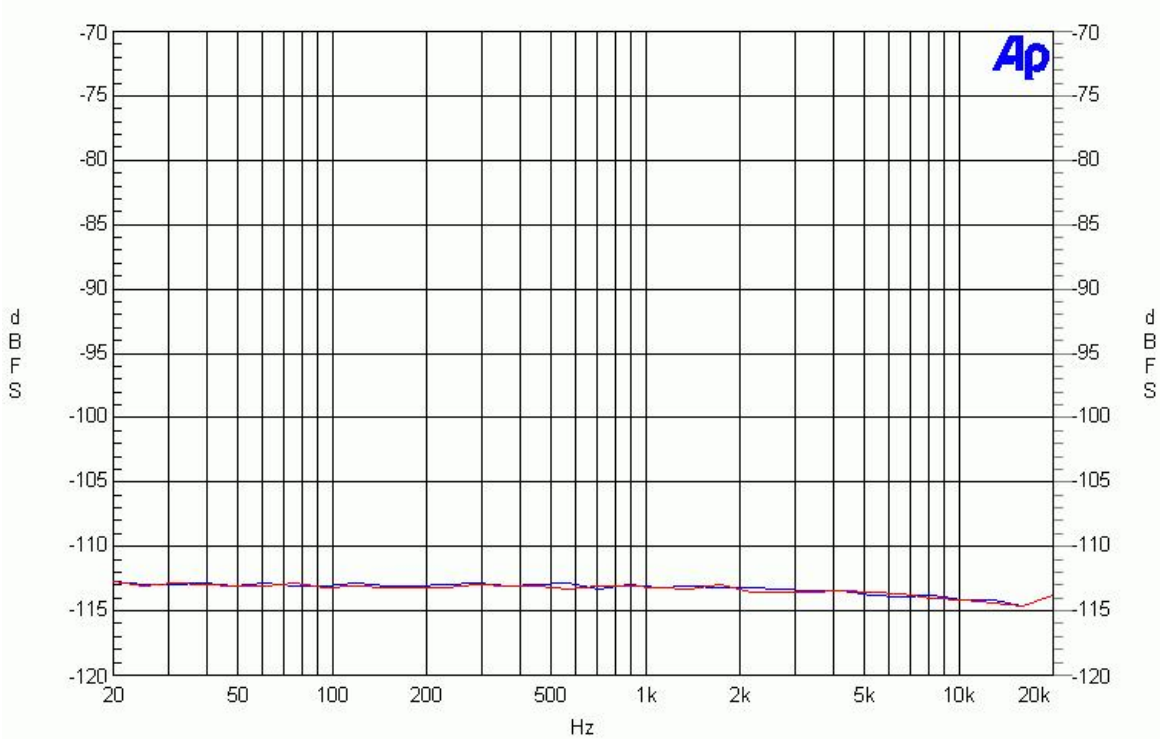
Measurement Plots 52-5250A



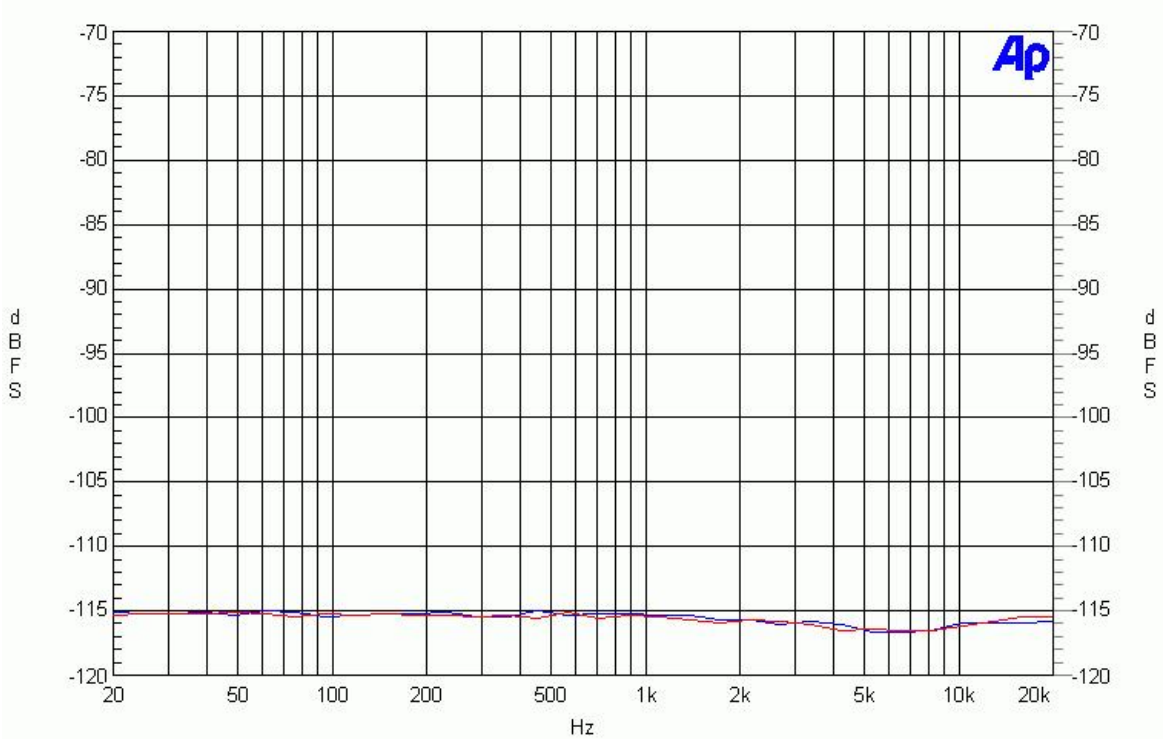
52-5250A Frequency Response, Pad OFF



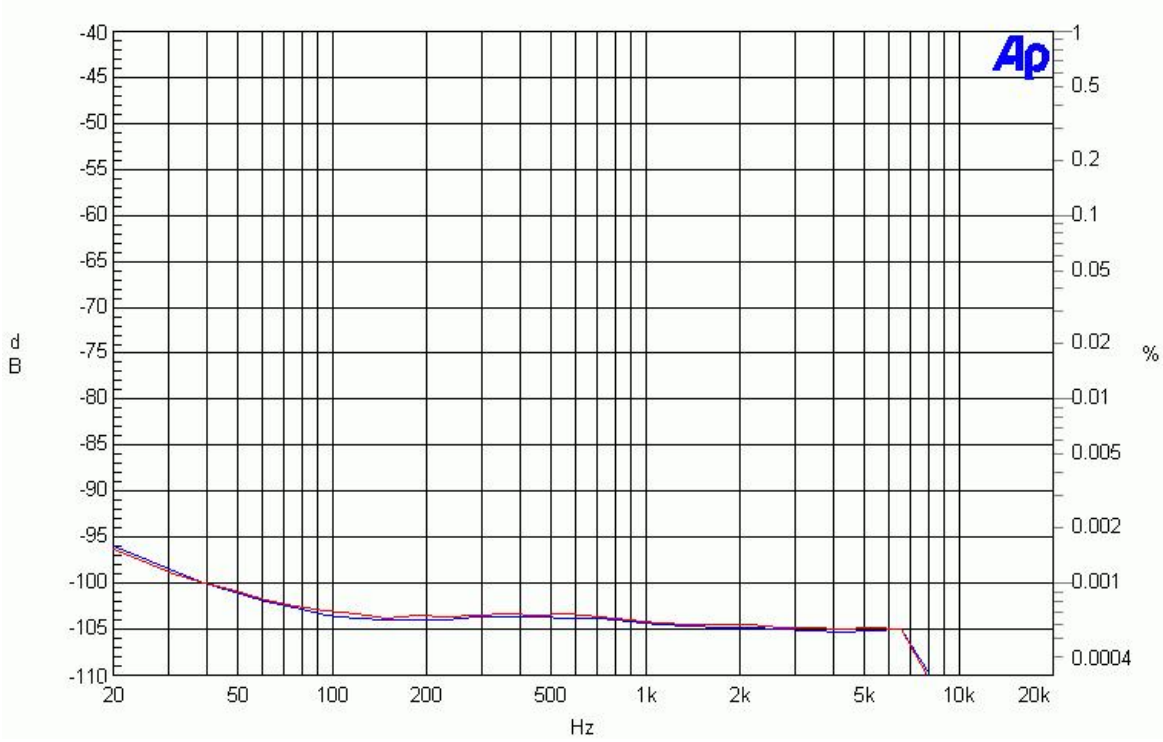
52-5250A Frequency Response, Pad ON



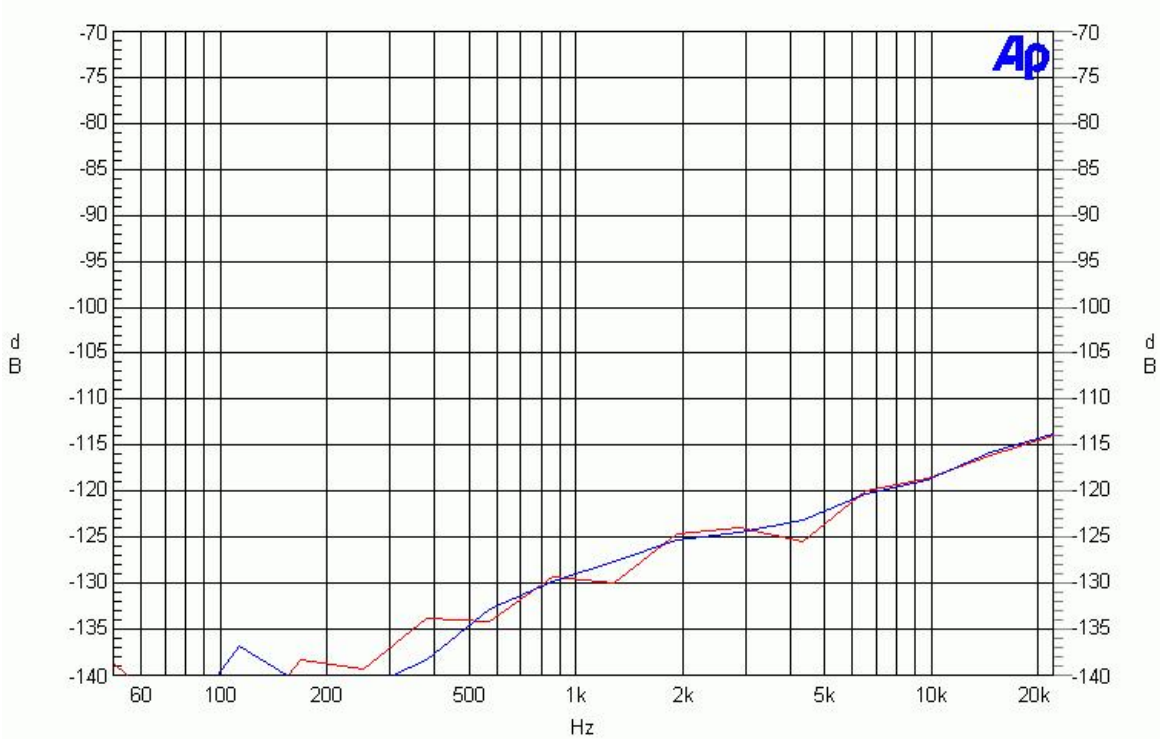
52-5250A THD+N @ -30 dBFS



52-5250A THD+N(A) @ -30 dBFS



52-5250A THD+N @ +14 dBu



52-5250A Cross-Talk

Log File Example

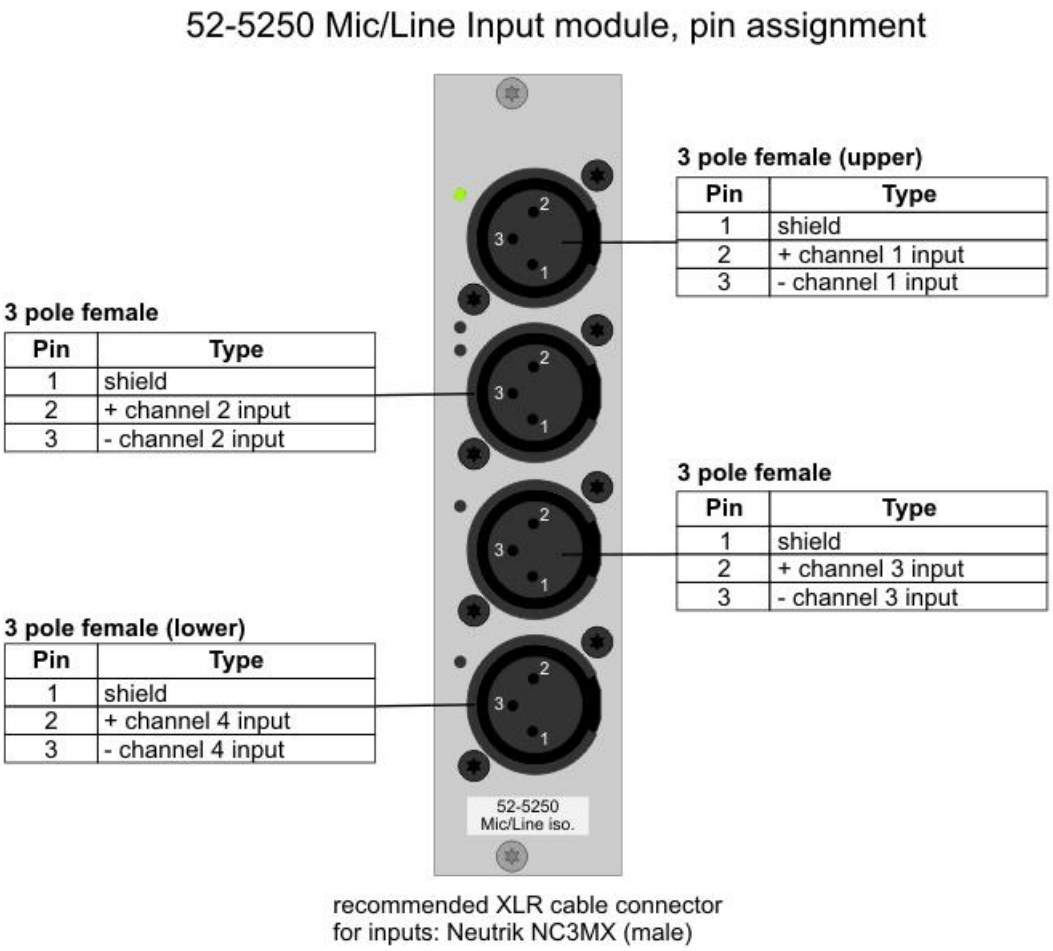
After manufacturing all inputs and outputs of every I/O card are measured. Hence, we can make sure that every module, leaving the production hall, is working correctly. During this process a log file is written. This file is saved by DHD for maintenance purposes.

In the following you can find a log file example of an 52-5250 module:

```
test protocol: z52-52502
serial number: 606442110
production code: 6442
test date: 02-May-2007 13:14:38

frequency response (abs.max. ripple 20Hz..20kHz)
Limit: -0.05 dB .. +0.02 dB
  Ch1: 0.02 dB
  Ch2: 0.01 dB
  Ch3: 0.02 dB
  Ch4: 0.01 dB
ADC dynamic range:
Limit: +110 dB .. +Inf dB
  Ch1: 113.1 dB
  Ch2: 113.0 dB
  Ch3: 113.1 dB
  Ch4: 113.1 dB
ADC multitone distortions and noise:
Limit: -Inf dB .. -98 dB
  Ch1: -110.4 dB
  Ch2: -110.0 dB
  Ch3: -109.8 dB
  Ch4: -109.8 dB
equivalent input noise (60 dB Gain, 200 Ohm source):
Limit: -Inf dBu .. -125 dBu
  Ch1: -127.2 dBu
  Ch2: -127.4 dBu
  Ch3: -127.5 dBu
  Ch4: -126.9 dBu
common mode rejection (20Hz..15kHz, worst case):
Limit: 60 dB .. Inf dB
  Ch1: 98 dB
  Ch2: 88 dB
```

```
  Ch3: 90 dB
  Ch4: 94 dB
power supplies:
  VCC1V2: 1.22 V
  VCC2V5: 2.55 V
  VCC3  : 3.27 V
  VCC5  : 5.02 V
  VPHANTOM: 46.1 V
```

Pin Assignment



Pin out for the 52-5250 Module.

52-5260A - MB/CR/XD 4 Line Out Module, iso.

Technical Specifications

D/A Converter

max. output level (phones, single ended):	18 dBu (balanced)
output impedance:	approx. 32 Ohm
minimum load (outputs short circuit protected):	600 Ohm
frequency response:	< 0.1 dB
THD+N:	< -108 dBFS (-30 dBFS, -15 dBu test signal level), (< -93 dBu)
	< -103 dBFS (-9 dBFS, +6 dBu test signal level), (< -88 dBu)
	< -90 dBFS (-1 dBFS, +14 dBu test signal level), (< -75 dBu)
crosstalk:	< -115 dB
dynamic range:	111 dB (A-weighted, 0 dBFS = +15 dBu)
DC offset voltage:	< 30 mV
common mode rejection (output impedance):	> 60 dB
common mode rejection (output voltage):	> 40 dB
converter technology:	24 bit, oversampling sigma-delta

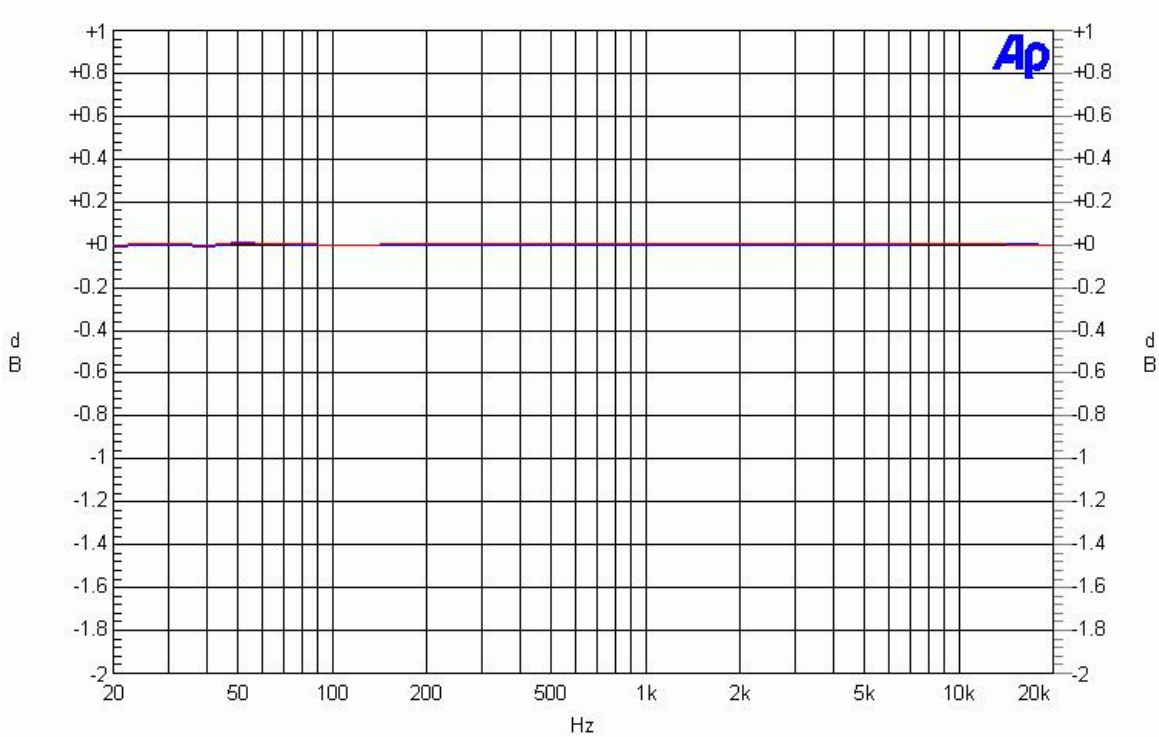
Further Information

power consumption:	2.9 (typical)
connector style:	XLR 3-pin connectors
printed circuit board (PCB) revision for this specifications:	1

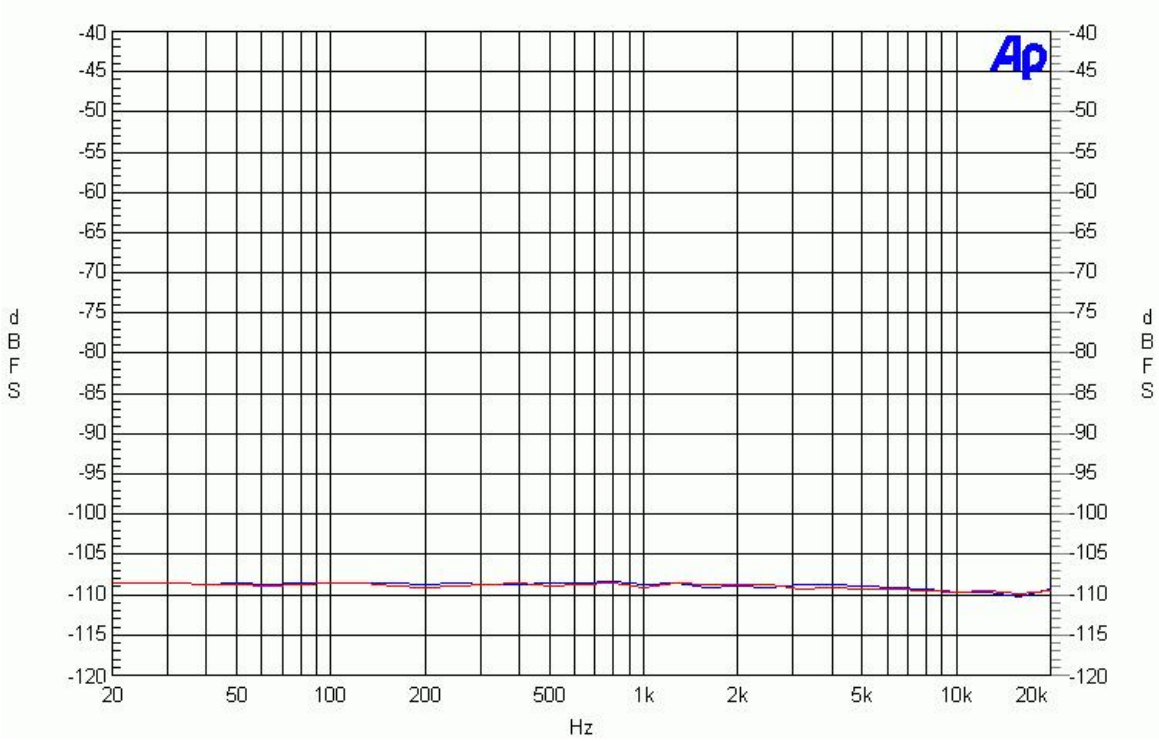
Note

All values are typical values, regarding the factory test limits, you can find in the log file example.

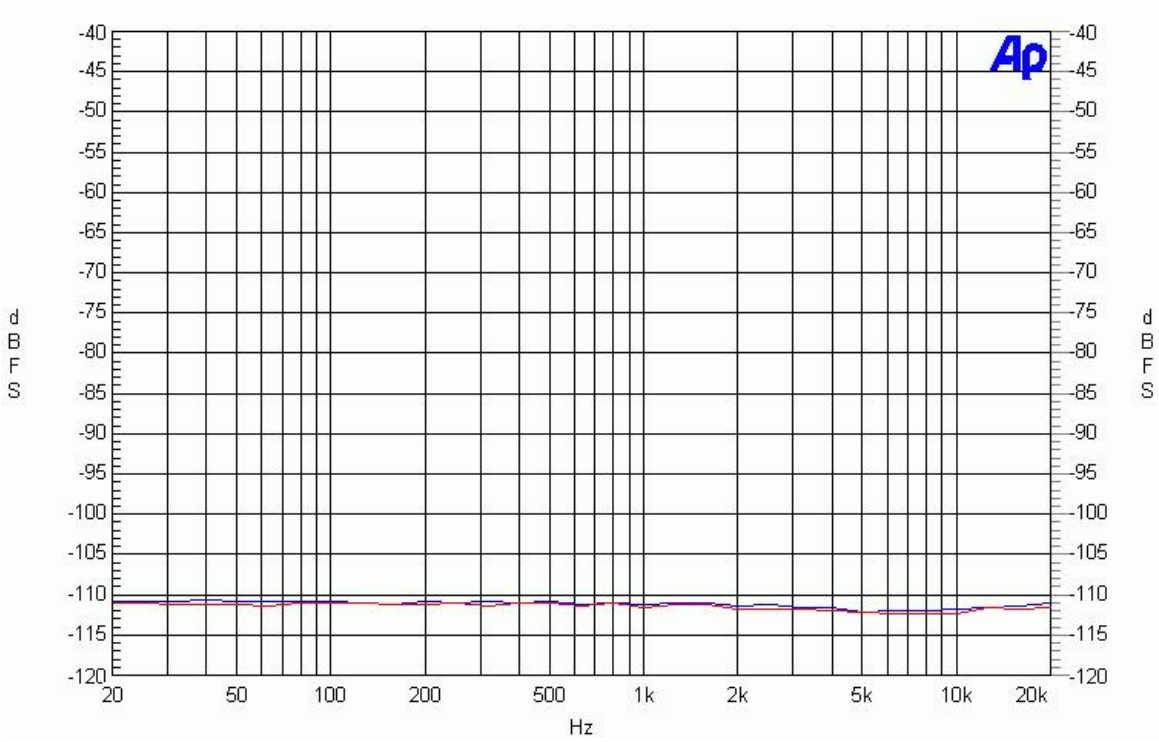
Measurement Plots 52-5260A



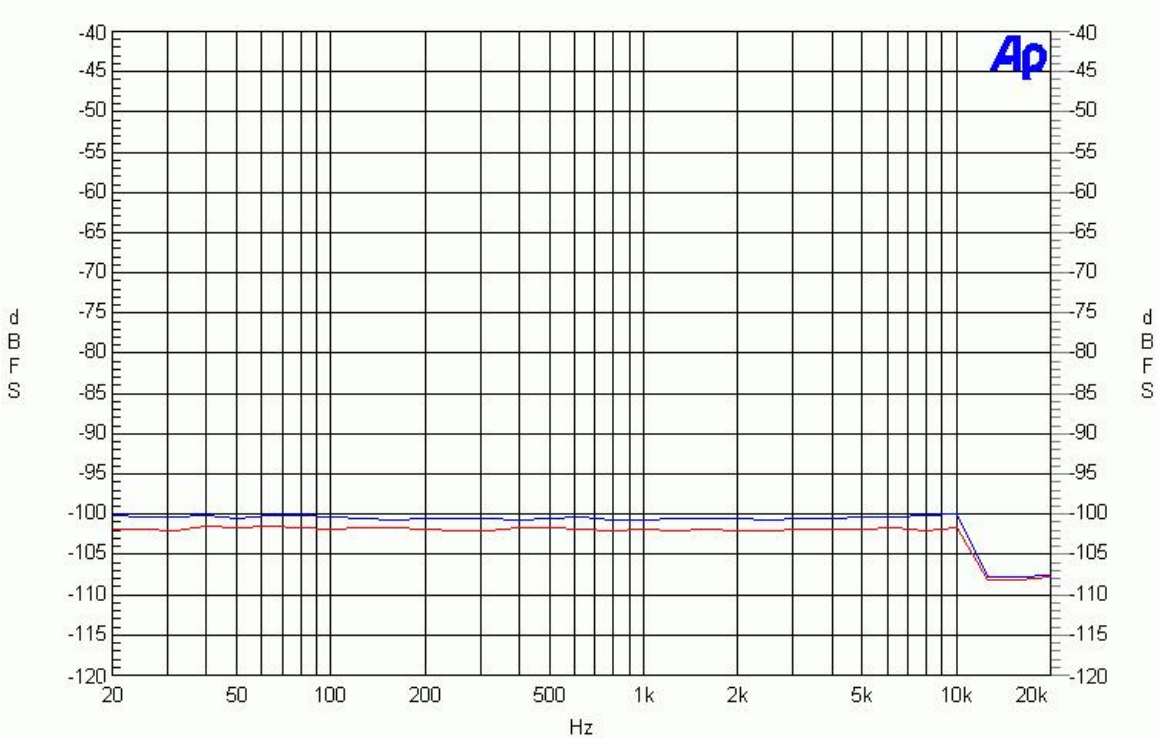
52-5260A Frequency Response



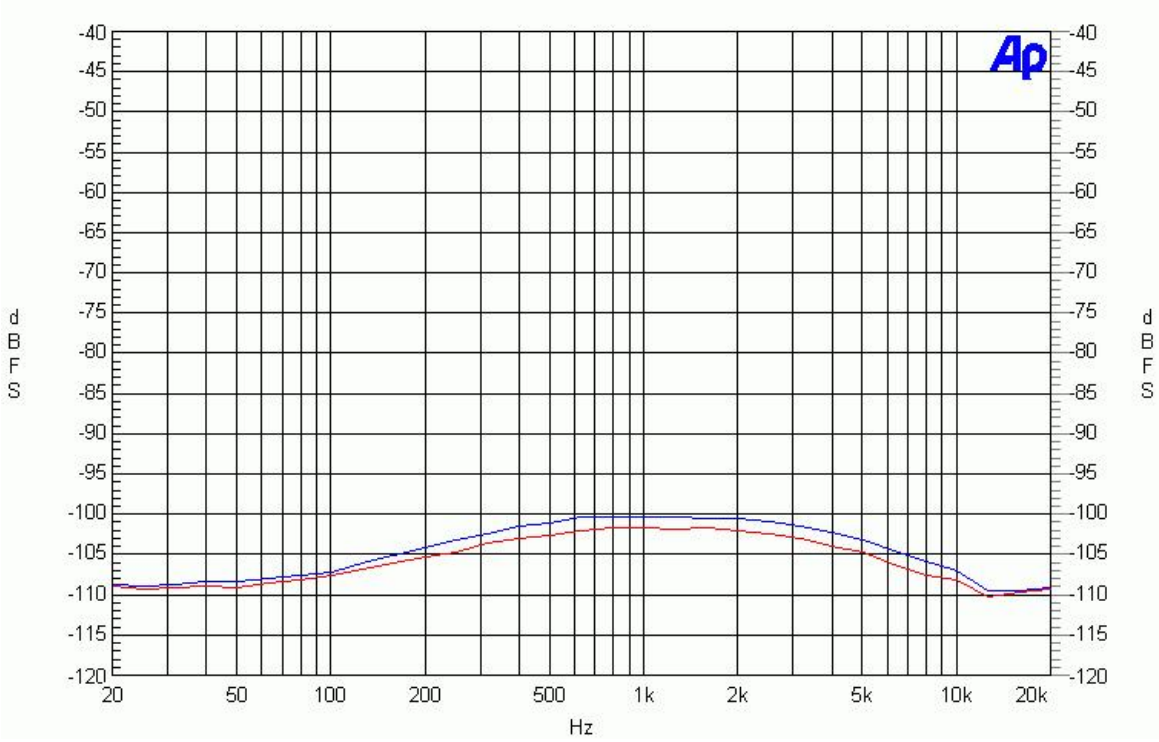
52-5260A THD+N @ -30 dBFS



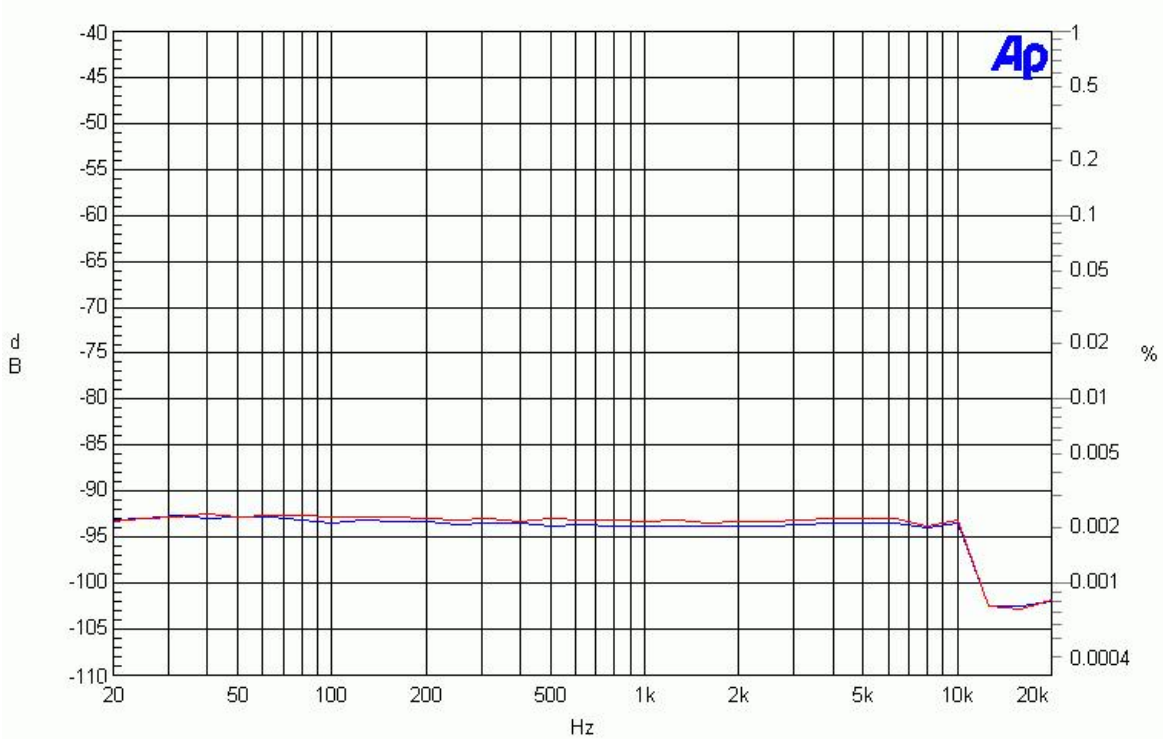
52-5260A THD+N(A) @ -30 dBFS



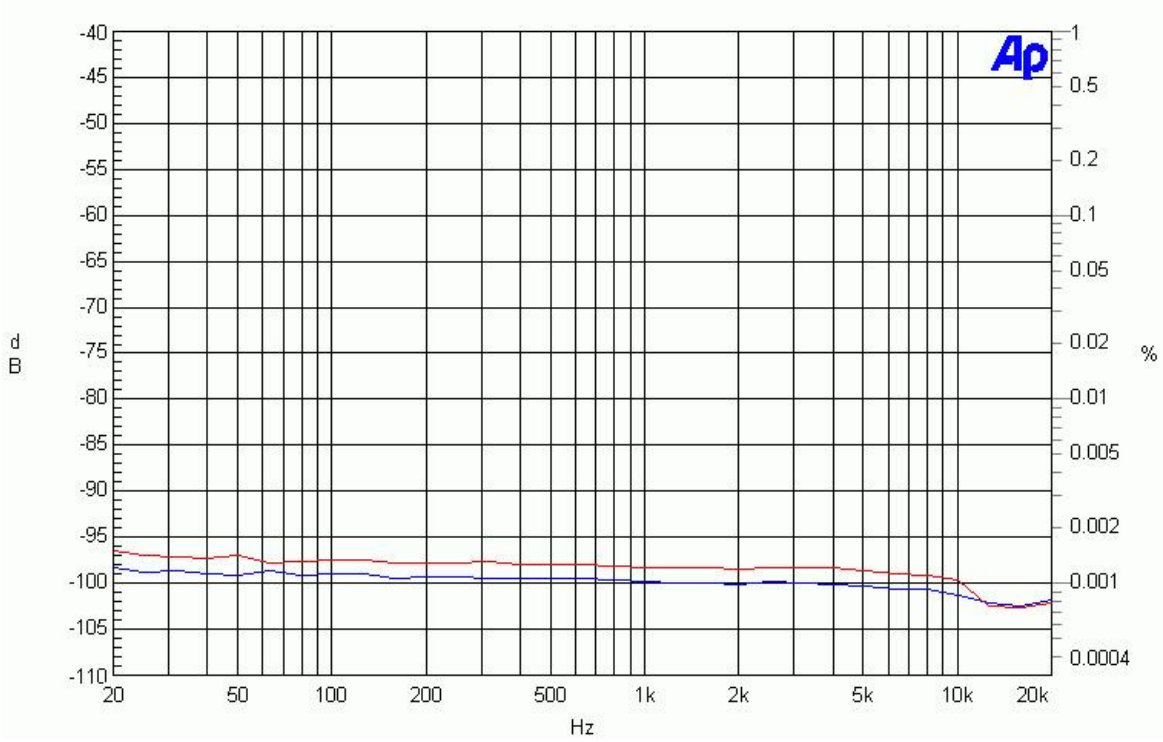
52-5260A THD+N @ +6 dBu, 600Ohm



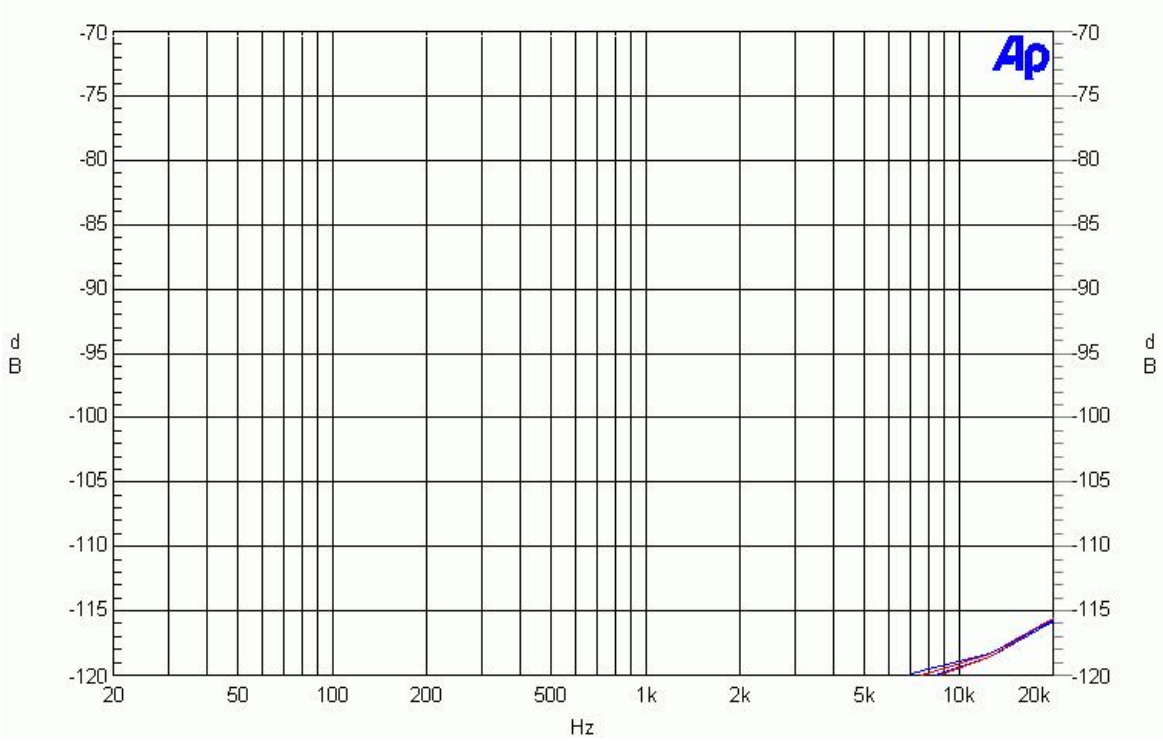
52-5260A THD+N(A) @ +6 dBu, 600Ohm



52-5260A THD+N @ +14 dBu, 600 Ohm



52-5260A THD+N @ +14 dBu, 100 kOhm



52-5260A Cross-Talk

Log File Example

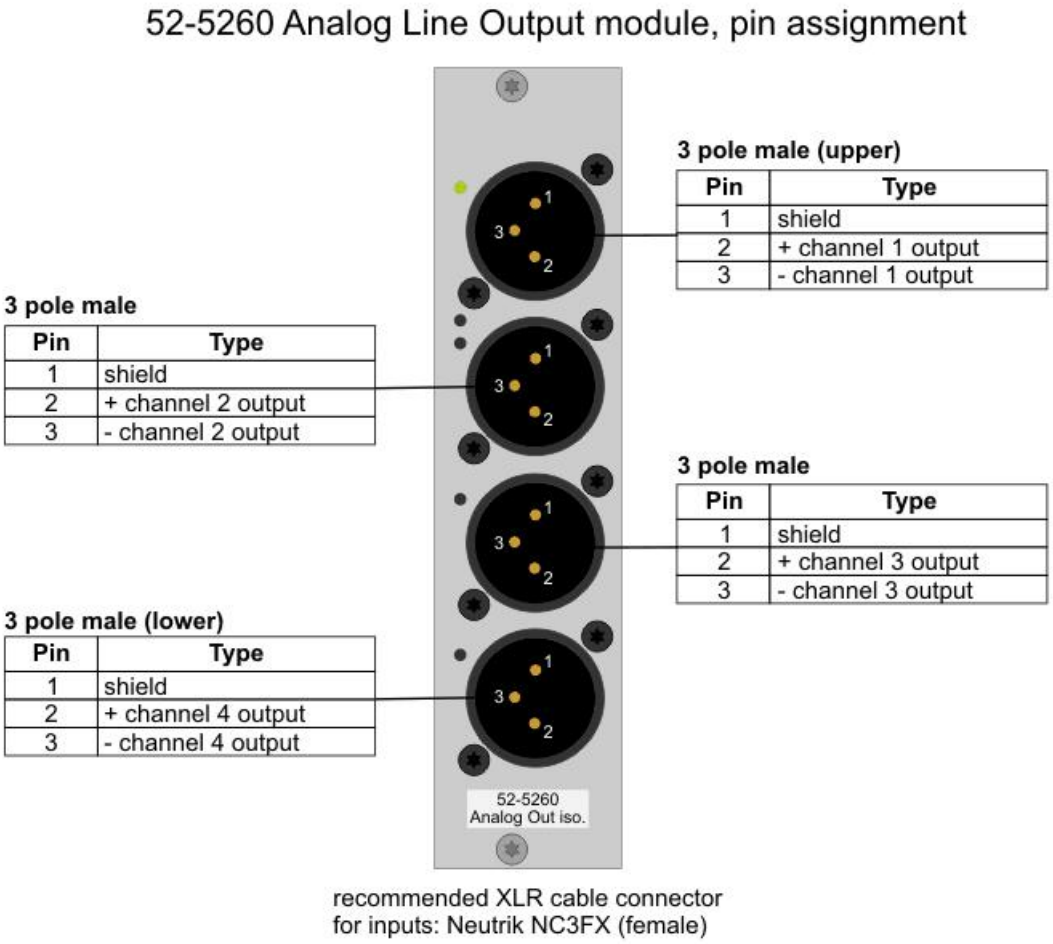
After manufacturing all inputs and outputs of every I/O card are measured. Hence, we can make sure that every module, leaving the production hall, is working correctly. During this process a log file is written. This file is saved by DHD for maintenance purposes.

In the following you can find a log file example of an 52-5260 module:

```
test protocol: z52-52601
serial number: 85
production code: 5430
test date: 02-May-2007 13:25:02

frequency response (abs.max. ripple 20Hz..20kHz)
Limit: -0.02 dB .. +0.02 dB
  Ch1: 0.01 dB
  Ch2: 0.01 dB
  Ch3: 0.01 dB
  Ch4: 0.01 dB
dynamic range:
Limit: +109 dB .. +Inf dB
  Ch1: 112.3 dB
  Ch2: 112.4 dB
  Ch3: 112.1 dB
  Ch4: 112.4 dB
DAC multitone distortions and noise (300 Ohm load):
Limit: -Inf dB .. -96 dB
  Ch1: -100.3 dB
  Ch2: -99.6 dB
  Ch3: -101.0 dB
  Ch4: -101.3 dB
output impedance:
  Ch1: 30.9 Ohm
  Ch2: 30.7 Ohm
  Ch3: 30.9 Ohm
  Ch4: 30.8 Ohm
common mode rejection (20Hz..15kHz, worst case):
Limit: 55 dB .. Inf dB
  Ch1: 60 dB
  Ch2: 59 dB
  Ch3: 67 dB
```

```
  Ch4: 56 dB
power supplies:
  VCC1V2: 1.23 V
  VCC2V5: 2.53 V
  VCC3  : 3.30 V
  VCC5  : 4.99 V
  AVCC  : 7.09 V
```

Pin Assignment



Pin out for the 52-5260 Module.

52-5310A - MB/XD/XR GPIO Module, 8 out, 4 in

Technical Specifications

General Purpose Inputs / Outputs (GPI/GPO)

4 GPIs (optocoupler, isolated):	external ON voltage 4 V ... 24 V (DC) without external resistor, internal current limiter to 4 mA current for ON, OFF voltage: 0 V ... + 1.5 V
8 GPOs (electronic relays, isolated):	maximum rated current: 0,2A (resettable fuse), maximum peak switched voltage: 30V AC or DC

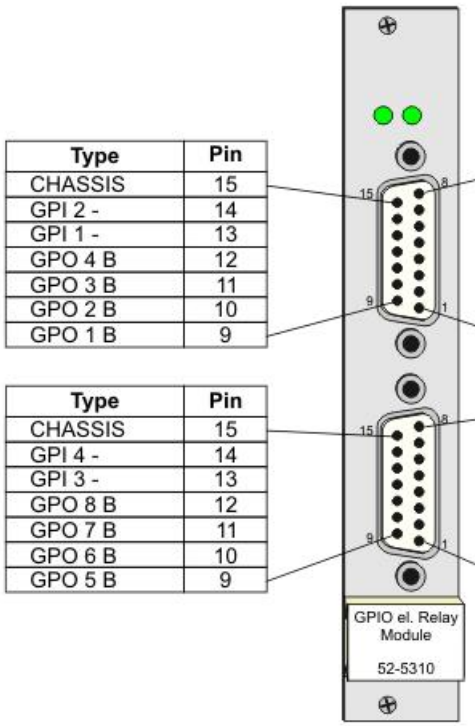
Further Information

power consumption:	1 W (typical)
connector style:	2 SubD-15 connectors
printed circuit board (PCB) revision for this specifications:	1

Note

All values are typical values, regarding the factory test limits.

Pin Assignment



Type	Pin
CHASSIS	15
GPI 2 -	14
GPI 1 -	13
GPO 4 B	12
GPO 3 B	11
GPO 2 B	10
GPO 1 B	9

Pin	Type	Address
8	Pot. 1	Pot. 1
7	V GPI 1/2	
6	GPI 2 +	GPI 2
5	GPI 1 +	GPI 1
4	GPO 4 A	GPO 4
3	GPO 3 A	GPO 3
2	GPO 2 A	GPO 2
1	GPO 1 A	GPO 1

Type	Pin
CHASSIS	15
GPI 4 -	14
GPI 3 -	13
GPO 8 B	12
GPO 7 B	11
GPO 6 B	10
GPO 5 B	9

Pin	Type	Address
8	Pot. 2	Pot. 2
7	V GPI 3/4	
6	GPI 4 +	GPI 4
5	GPI 3 +	GPI 3
4	GPO 8 A	GPO 8
3	GPO 7 A	GPO 7
2	GPO 6 A	GPO 6
1	GPO 5 A	GPO 5

"CHASSIS" meint, nur verbunden mit Gehäuse des Gerätes und Steckergehäuse, jedoch nicht mit der internen Schaltungsmasse, da galvanisch getrennt.

"CHASSIS" means wired to DSP frame enclosure and connector housing, but not to internal circuit ground of the module because it is galvanically isolated.

Pin out for the 52-5310 Module.

52-5311A - MB/XD/XR GPIO Module, 8 out, 4 in

Technical Specifications

General Purpose Inputs / Outputs (GPI/GPO)

4 GPIs (optocoupler, isolated):	external ON voltage 4 V ... 24 V (DC) without external resistor, internal current limiter to 4 mA current for ON, OFF voltage: 0 V ... + 1.5 V
8 GPOs (electromechanic relays, isolated):	maximum rated current: 1A (resettable fuse), maximum peak switched voltage: 30V AC or DC

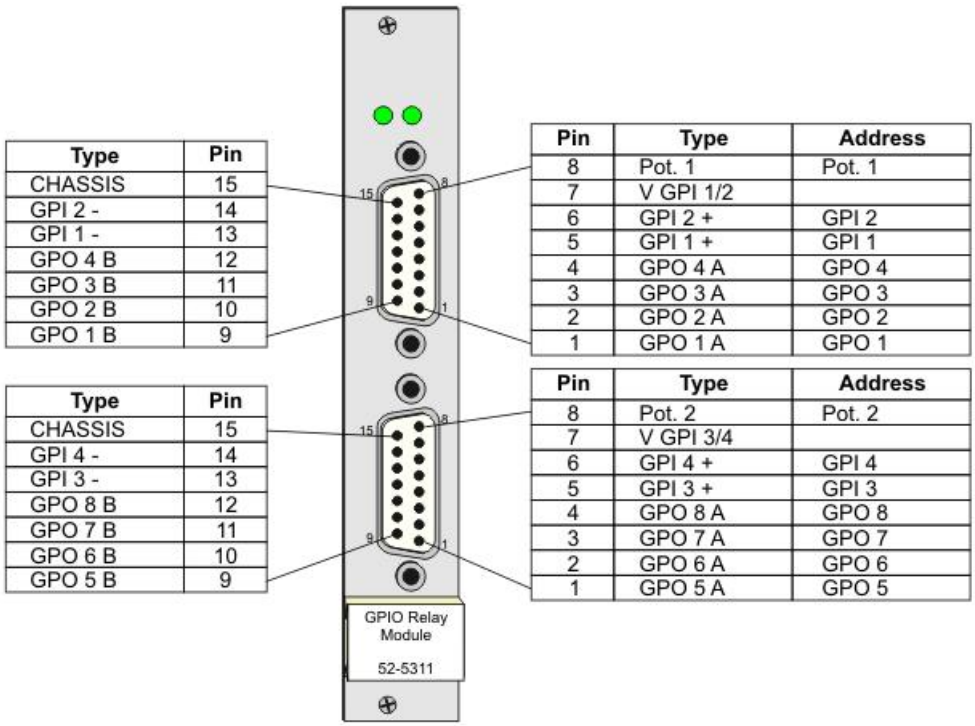
Further Information

power consumption:	1 W (typical)
connector style:	2 SubD-15 connectors
printed circuit board (PCB) revision for this specifications:	1

Note

All values are typical values, regarding the factory test limits.

Pin Assignment



Type	Pin
CHASSIS	15
GPI 2 -	14
GPI 1 -	13
GPO 4 B	12
GPO 3 B	11
GPO 2 B	10
GPO 1 B	9

Pin	Type	Address
8	Pot. 1	Pot. 1
7	V GPI 1/2	
6	GPI 2 +	GPI 2
5	GPI 1 +	GPI 1
4	GPO 4 A	GPO 4
3	GPO 3 A	GPO 3
2	GPO 2 A	GPO 2
1	GPO 1 A	GPO 1

Type	Pin
CHASSIS	15
GPI 4 -	14
GPI 3 -	13
GPO 8 B	12
GPO 7 B	11
GPO 6 B	10
GPO 5 B	9

Pin	Type	Address
8	Pot. 2	Pot. 2
7	V GPI 3/4	
6	GPI 4 +	GPI 4
5	GPI 3 +	GPI 3
4	GPO 8 A	GPO 8
3	GPO 7 A	GPO 7
2	GPO 6 A	GPO 6
1	GPO 5 A	GPO 5

"CHASSIS" meint, nur verbunden mit Gehäuse des Gerätes und Steckergehäuse, jedoch nicht mit der internen Schaltungsmasse, da galvanisch getrennt.

"CHASSIS" means wired to DSP frame enclosure and connector housing, but not to internal circuit ground of the module because it is galvanically isolated.

Pin out for the 52-5311 Module.

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